Integratie van optische interconnecties en opto-elektronische componenten in flexibele folies

Integration of Optical Interconnections and Optoelectronic Components in Flexible Substrates

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"Wie geen bom durft gooien, schrijve er één"
LOUIS PAUL BOON, AALST 1912-1979.

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Samenvatting

Licht als informatiedrager voor datacommunicatie heeft reeds vele jaren zijn succes bewezen. Lange afstands interconnecties tussen steden en continenten zijn tegenwoordig allen optisch. Over kortere afstanden, zoals interconnecties van chip tot chip op eenzelfde printkaart, staan optische verbindingen ook al reeds ruime tijd in de kijker en hebben ze al meermaals bewezen een oplossing te kunnen bieden voor de nakende tekortkomingen van elektrische verbindingen. Aanvaarding van optische verbindingen op de printkaart op een commerciele schaal laat echter nog op zich wachten. Hoewel de gerapporteerde performantie van optiche printkaartverbindingen steeds toeneemt, blijven de industriele toepassingen van dit principe beperkt tot nichedomeinen.

Dit doctoraatsonderzoek introduceert optische verbindingen in een van de sterkst groeiende segmenten binnen de elektronica op dit moment, namelijk de markt van de flexibele elektronica. Door de optische verbindingen en alle toebehorende actieve en passieve elementen zeer dun en plooibaar te maken, kunnen we ze integreren in een dunne flexibele folie. Dit opent een waaier aan mogelijke toepassingen in draagbare elektronica waar de flexibele substraten nu al domineren. In auto-, vliegtuig- , ruimte- en medische toepassingen hebben optische vezel communicatie en flexibele elektronica al lang hun doorbraak gemaakt, voornamelijk gedreven door hun lage gewicht en hoge graad van compactheid. De immuniteit tegen elektromagnetische interferentie en bestendigheid tegen extreme omstandigheden van optische vezels zijn ook veel gestelde vereisten binnen deze sectoren. De flexibele optische verbindingen in dit doctoraatsonderzoek kunnen de bovengenoemde elektrische en optische netwerken combineren in *éé*n enkel systeem.

Licht vindt niet alleen toepassing als digitale informatiedrager voor data communicatie, maar ook als analoge informatiedrager in optische sensoren, welke een heel gamma aan chemische, biologische en fysische variabelen kunnen detecteren en kwantificeren. Optische sensoren bezitten enkele toonaangevende voordelen vergeleken met hun elektrische tegenhangers met een grote groei in dit onderzoeksdomein als gevolg. Sensoren moeten weliswaar in vele gevallen

zo compact mogelijk zijn en een zo laag mogelijke impact hebben op het systeem design. De hoge graad van integratie die in dit werk wordt bereikt, kan de grootte en de kost van bestaande optische sensoren wezenlijk verlagen en daardoor ook de meetpuntdensiteit verhogen.

De integratie van opto-elektronische componenten, optische golfgeleiders en koppelstructuren in een 150 μm dunne flexibele folie bewijst niet alleen zijn nut in flexibele elektronica en optische sensoren, maar brengt ook een toegevoegde waarde aan de huidige kennis en mogelijkheden omtrent bestaande optische verbindingen op printkaart, zoals hoger beschreven. De hoge graad van integratie minimaliseert de plaats die de interconnectie inneemt op de printkaart of kan ze zelfs herleiden tot nul. De mechanische flexibiliteit verhoogt de betrouwbaarheid van de interconnectie, de dunheid van de folie maakt 3D stapelen van meerdere interconnectiefolies op elkaar mogelijk en de hoge functionaliteit van de folie met slechts een elektrische interface naar buiten, kan de aanvaarding van optische verbindingen op printkaart aanzienlijk versnellen. Een meer gedetailleerde beschrijving van de toepassingsmogelijkheden van de optische folie wordt gegeven in hoofdstuk 1.

Een nieuwe generatie optische golfgeleiders realiseren door ze flexibel te maken, brengt heel wat technologische uitdagingen met zich mee. Het materiaal voor de optische golfgeleiders moet beschikken over een uitstekende flexibiliteit en weerstand tegen veelvuldig plooien. De huidige markt van optische materialen groeit zeer snel, maar de commerciele verkrijgbaarheid van meeste materialen is nog steeds problematisch. Hoofdstuk 2 zet de materiaalvereisten uiteen, geeft een overzicht van de bestaande optische polymeren en mogelijke modificaties aan deze materialen.

De meest toegepaste vorm van lichtgeleiding op printkaarten is het gebruik van polymere optische golfgeleiders dankzij hun vele voordelen en veelzijdige fabricagemogelijkheden. Hoofdstuk 3 beschrijft de gebruikelijke technologie$\ddot{e}$n voor het vervaardigen van golfgeleiders gevolgd door een intense studie van fotolithografische golfgeleiders met speciale aandacht voor het aanbrengen van de lagen, het uitbakken, de laaguniformiteit, de reproduceerbaarheid, het golfgeleiderprofiel, de zijwandruwheden en de planarisatie. De focus ligt vooral op de controle over de dimensies van de golfgeleiderlagen aangezien de dunne optoelektronische componenten en optische koppelstructuren hierin zullen worden ingebed met hoge alignatievereisten. Met deze belangen in gedachten werd het golfgeleider fabricageproces geoptimaliseerd voor verschillende materialen: Truemode™ Backplane Polymer , LightLink™ , Epocore / Epoclad en Ormocers® . Problemen als edge bead, onderlinge adhesie, luchtbellenincapsulatie, proximity UV belichting and golfgeleider T-topping worden bestudeerd en naar mate van het mogelijke ge$\ddot{e}$limineerd.

In hoofdstuk 4 worden methoden voorgesteld voor het verwezenlijken van flexibele golfgeleiders. De golfgeleiderstructuur wordt mechanisch versterkt met behulp van extra Polyimide lagen. Op deze manier kunnen de anders breekbare lagenstructuren zonder problemen gebogen worden. Drie verschillende methoden worden onderzocht: het fabriceren van golfgeleiders bovenop een Polyimide folie, het lamineren van afgewerkte golfgeleiders tussen twee Polyimide folies en het spincoaten van Polyimide lagen en golfgeleiderlagen in *éé*nzelfde proces. Gezien de onhandelbaarheid van flexibele substraten wordt een methode ontwikkeld om de gehele fabricage te laten verlopen op een tijdelijk rigide drager. Achteraf kan de rigide drager op een eenvoudige wijze verwijderd worden. De flexibiliteit en de optische buigingsverliezen van de bekomen golfgeleiderfolie worden onderzocht. Metingen wijzen het Truemode™ Backplane Polymer materiaal aan als meeste flexibel onder de onderzochte materialen met een minimale buigingsradius van 2.5 mm, getest over 1000 buigingscycli. De gemeten optische buigingsverliezen van de flexibele LightLink™ en Truemode™ Backplane Polymer golfgeleiders zijn vergelijkbaar met de in de literatuur gerapporteerde waarden.

Commercieel verkrijgbare Gallium Arsenide opto-elektronische componenten zijn te dik om te worden ingebed in een dunne folie. In hoofdstuk 5 presenteren we een mechanisch verdunningsproces voor individuele chips voor de realisatie van ultradunne (20 μm) opto-elektronische componenten. Mechanische en optische karakterisatie toont aan dat de integriteit en functionaliteit van de componenten ongewijzigd blijft tijdens het verdunningsproces. Mechanische stress in de GaAs chips is geminimaliseerd door optimalisatie tot een rms ruwheid lager dan 10 nm, gemeten over een gebied van 200 x 200 μm^2. De vlakheid van de gepolijste zijde van de finale componenten is lager dan 2 μm na optimalisatie van het fixeren van de chips voor het verdunnen. Bovendien is de voorgestelde technologie schaalbaar tot GaAs chips met een grootte tot 10 x 10 mm^2.

Het volledig inbedden van de verdunde opto-elektronische componenten in de flexibele optische folie is beschreven in hoofdstuk 6. Verschillende polymeren werden getest op hun geschiktheid als inbeddingsmateriaal. Gezien sommige componenten zoals VCSEL's veel warmte kunnen genereren, wordt een koperen eiland voor warmteafvoer voorzien ter hoogte van elke chip. Laser geableerde via's en ingebedde gesputterde koperbaantjes zorgen voor galvanisch contact naar de contactpaden van de ingebedde componenten. Contacten naar de buitenwereld worden geopend met verschillende opeenvolgende laser ablatie stappen, waarna de geopende contactpaden kunnen worden gesoldeerd of opgeplate met Ni-Au. Om de intelligentie en functionaliteit van de folie te vergroten, worden IC's (geintegreerde circuits) ingebed in dezelfde laag als de opto-elektronische chips. Alignatie van de golfgeleiders ten opzichte van de componenten gebeurt

met standaard lithografie met positioneringsjuistheid binnen de 10 μm .

VCSEL's en fotodiodes zijn vertikaal emitterende en detecterende elementen in tegenstelling tot de golfgeleiders welke horizontaal zijn gepositioneerd. Om dit probleem te verhelpen, zijn 90 graden koppelstructuren noodzakelijk. Deze veroorzaken wel een groot deel van de totale optische verliezen van het systeem en moeten met veel zorg gekozen worden. In hoofdstuk 7 worden de simulaties, fabricagemethodes en karakterisatie van twee verschillende aanpakken met elkaar vergeleken: laser geableerde spiegels en discrete spiegelcomponenten. In simulaties met ZEMAX ray tracing software ontrafelen we en kwantificeren we de verschillende factoren die bijdragen tot het totale optische vermogenverlies in de optische folie. Verschillende fabricage methodes voor de discrete spiegelcomponent worden ontwikkeld en besproken. Deze spiegelcomponenten worden ingebed en gealigneerd ($\pm$10 μm positionering) in de lagenopbouw van flexibele optische folie. Optische communicatie naar de buitenwereld van en naar de folie is mogelijk gemaakt door het inbedden en aligneren van naakte optische glasvezels, waardoor het gebruik van lijvige connectoren overbodig wordt gemaakt.

Teneinde de performantie van de ontwikkelde inbeddingstechnologie te bestuderen, worden demonstratorfolies gemaakt, bestaande uit 4 ingebedde parallelle 2 cm lange golfgeleiderverbindingen tussen een 20 μm dunne 1 x 4 VCSEL rij en een 1 x 4 fotodiode rij met een pitch van 250 μm. In hoofdstuk 8 wordt het optische vermogenbudget, de optische overspraak, de mechanische flexibiliteit, het hoogfrequentgedrag, de betrouwbaarheid en het warmtemanagement van deze demonstrator gekarakteriseerd en besproken. Verschillende optische meetopstellingen worden doorgevoerd om na te gaan welke factoren de grootste bijdrage leveren bij de totale optische verliezen. De totale verliezen over heel de link bedragen 20 dB $\pm$ 7 dB bij het gebruik van laser geableerde spiegels en 6.4 dB $\pm$ 1.5 dB bij het gebruik van ingebedde discrete spiegelcomponenten. De overspraak tussen twee naburige golfgeleiderkanalen met een lengte van 8 cm bedraagt -34 dB, terwijl de overspraak tussen 2 naburige VCSEL-tot-fotodiode linken -17 dB bedraagt. Vervolgens wordt de buigbaarheid bestudeerd van zowel de flexibele golfgeleiders, de ingebedde opto-elektronische componenten als van de flexibele demonstratorlink. Een rigide optische link met aangepast elektronisch ontwerp op een rigide substraat werd samengesteld om tijds- en frekwentiedomein karakterisatie te doen met standaard 50 Ohm meetapparatuur, resulterend in een open oog diagram bij 1.2 Gb/s. De flexibele optische links werden samen met rigide optische links aan betrouwbaarheidstesten onderworpen, bestaande uit stockage-, warmte- en vochtbestendigheidstesten. De flexibele links vertonen geen tekenen van achteruitgang na 100 temperatuurscycli tussen -40^{o}C and + 125^{o}C en na 1000 uur op 85 ^{o}C bij een relatieve luchtvochtigheid van 85 %, in tegenstelling tot de rigide links, welke stuk voor stuk achteruitgin-

gen. Het thermische management van ingebedde VCSEL's wordt geanalyseerd met een 2D doorsnedemodel en een dunneplaatmodel. Verdere optische karakterisatie van gewirebonde VCSEL's en ingebedde VCSEL's toont aan dat het inbedden geen invloed heeft op de optische eigenschappen van de VCSEL's.

Ten laatste worden in hoofdstuk 9 de voornaamste conclusies op een rijtje gezet en worden toekomstig werk en opportuniteiten toegelicht.

Summary

Light as a transmission medium for data communication has proven its success for many years. Over long distances like intercontinental and intercity links, optical interconnects have been the obvious choice due to the low propagation losses and high bandwidth. Over short distances, optical data communication on board has drawn a lot of attention and has proven to bring a solution to the emerging bottle necks of electrical interconnects, but adaption of this technology on a commercial scale has still not been conveyed. As the demonstrated performance of optics on board is higher every year, the adaption in the industry is still predetermined for niche applications.

This PhD work addresses the introduction of on-board optical communication in one of the fastest growing market segments in electronics today: the flexible substrate electronics. By making the optical interconnects and every accompanying active and passive feature very thin and flexible, we can integrate everything in a thin bendable foil. This opens a world of opportunities in portable and wearable applications were flexible electronics are already dominating today. In automotive, avionics, aero-space and medical applications, optical fiber communication and flexible electronics have made their break-through long time ago, mainly driven by the low weight and compactness of both and the immunity to electromagnetic interference and reliability in harsh environments of optics. The flexible optical interconnections presented in this PhD research combine the electrical and optical network into one system.

Light is presented here as the carrier of bit data, but in an analog point of view, light can be used for sensing a wide range of chemical, biological and physical parameters. Optical sensor system have shown some main advantages over their electrical counterparts with a large growth in this research area as a consequence. As sensors often need to be as compact and unobtrusive as possible, the high level of integration reached in this PhD work can significantly reduce the size, measurement point pitch and cost of existing optical sensors.

The integration of opto-electronics, optical waveguides and coupling structures

in a 150 μm thin flexible foil presented in this thesis can not only find its application in flexible electronics and optical sensors, but brings an additional value to the state-of-the-art of existing on-board rigid interconnects discussed above. Namely, the high level of integration can significantly reduce or even eliminate the footprint of the interconnections, the mechanical flexibility can improve the reliability, the thinness of the foil enables 3D stacking of interconnects and the stand-alone nature of the optical link foil can fasten up the industry acceptance of optics on-board. A more detailed description on these advantageous aspects of the presented optical foil will be given in Chapter 1.

Taking polymer optical waveguides to a next generation by making them flexible, brings on some additional technological challenges. The optical waveguide material needs to prove excellent bending behavior and endurance. The existing optical material market is rapidly expanding, though commercial availability still is a major drawback. Chapter 2 puts apart the material requirements, the state-of-the-art materials and gives a view on the possible modification of existing materials.

The most popular optical interconnection approach on board is the use of waveguides due to their many advantages and versatile fabrication methods. Chapter 3 summarizes and discusses the different waveguide fabrication possibilities followed by an intense study of photolithographic waveguides, with special attention to layer deposition, curing, layer uniformity, reproducibility, waveguide profile, side wall roughness and planarization. The main focus lies on the good control over the waveguide stack dimensions, since active components and coupling elements will be integrated herein with high positioning requirements. With these concerns in mind, the process steps in the fabrication process of waveguides in Truemode™ Backplane Polymer , LightLink™ , Epocore / Epoclad and Ormocers® material were optimized and problems like edge bead, adhesion issues, air bubble insertions, proximity mode UV exposure and waveguide T-topping were studied and tackled within the possibilities.

Chapter 4 takes the principle of optical polymer waveguides on board to an other dimension. The waveguide layer stack is adjusted to allow the waveguides to be bended. Polyimide support layers offer the necessary strength and support for the otherwise not flexible optical waveguide materials. Three different approaches are investigated: the optical waveguide stack on top of a Polyimide foil, in between two spin-coated Polyimide layers and laminated between two Polyimide foils. Release techniques are developed to enable rigid processing of the flexible waveguides on a temporary rigid carrier with easy release afterwards. The resulting waveguide foils are investigated for their flexibility and optical bending propagation losses. Measurements show that the Truemode™ Backplane Polymer material shows superior bending behavior over the other

investigated materials with a minimum bending radius lower than 2.5 mm tested for 1000 bending cycles and that the bending losses of the LightLink™ and Truemode™ Backplane Polymer materials are comparable to those reported in literature.

Commercially available GaAs opto-electronic components are too thick to be embedded inside a thin foil. In Chapter 5, we will present a backside mechanical thinning process for individual dies for the realization of ultra thin (20 μm) optoelectronic components. Mechanical and optical characterization points out that their integrity and functionality is maintained after the thinning process. Mechanical stress inside the GaAS dies is minimized by optimization of the backside roughness to lower than 10 nm rms, measured in an area of 200 x 200 μm^2. The flatness of the final thinned dies is below 2 μm due to the optimization of the chip mounting before thinning. The thinning process is scalable to GaAs chip sizes upto 10 x 10 mm^2.

The full embedding of the thinned opto-electronic components inside the optical waveguide foil is presented in Chapter 6. The embedding was investigated using different polymers as embedding material. As VCSEL's can dissipate a lot of heat, heat sinks are fabricated in the layer build-up. Laser ablated micro-via's and embedded sputtered copper tracks provide galvanic interconnection towards the embedded chips contact pads. Contacts to the outer world are opened using different laser ablation steps and can be soldered or Ni-Au plated afterwards. To enhance the intelligence and functionality of the foil, ultra thin Integrated Circuits (IC's) are embedded in the same layer as the opto-electronics. The waveguides are aligned with respect to the active with standard lithography processes, resulting in an alignment accuracy lower than 10 μm .

VCSEL's and Photodiodes are vertical emitting/detecting opto-electronics, while the embedded waveguides are a horizontally optical transportation medium. To overcome this, 90 degree out-of-plane coupling elements are needed. These elements have a large contribution to the total optical loss of the system and need to be chosen carefully. Chapter 7 investigates and compares the simulation, fabrication and characterization of two mirror approaches: laser ablated micro-mirrors and pluggable mirror inserts. Ray tracing ZEMAX simulations are performed to define the main dimensional contributors to the total optical loss of the system. Different fabrication processes for pluggable micro-mirrors are presented and compared. The mirror plug components are integrated and aligned with 10 μm accuracy inside the layer build-up of the optical waveguide foil. Optical communication to the outer world, from and towards the foil, is made possible by embedding and aligning single bare optical fibers inside the foil, eliminating the need for a bulky, rigid connector units.

To investigate the performance of the presented flexible active optical interconnections principle, a demonstrator is put forward consisting of four 2 cm long parallel VCSEL-to-Photodiode waveguide links between a 20 μm thin 1 x 4 VCSEL array and a 1 x 4 PD array with a pitch of 250 μm. In Chapter 8, the optical power budget, optical crosstalk, mechanical flexibility, high-frequency behavior, reliability and heat management of the demonstrator are characterized and discussed. Different measurements set-ups are assembled to define the major contributors to the total optical link loss and to compare the use of laser ablated mirrors and mirror plugs. The total optical link loss using laser ablated mirrors is 20 dB $\pm$ 7 dB, and using mirror plugs: 6.4 dB $\pm$ 1.5 dB. Crosstalk measurements show a cross-talk of -34 dB between two neighboring 8 cm long planar waveguides and -17 dB between two neighboring 2 cm long VCSEL-to-PD links. The flexible behavior of the waveguide stack, the opto-electronic package stack and the total active optical link are tested and compared. A special electronic design on a rigid optical embedded link was made to do time and frequency domain characterization using standard 50 Ohm test equipment resulting in a clear open eye diagram at 1.2 Gb/s. The reliability of the flexible optical link was investigated through storage, heat cycling and humidity tests. Temperature cycling and humidity cycling was performed on both rigid optical links on FR-4 and on flexible optical links. The flexible optical links do not degrade after 100 temperature cycles between -40^{o}C and + 125^{o}C and after 1000 hours at 85 ^{o}C at a relative humidity of 85 % in contrast to the total failure of their rigid counterparts. The thermal management of embedded VCSEL's is analyzed with a 2D cross-sectional model and a thin plate model. Optical characterization and comparison of wire-bonded VCSEL's and embedded VCSEL's shows that the embedding does not influence the optical behavior of the VCSEL's.

Finally, the main conclusions and a look on future work and opportunities will be discussed in Chapter 9.

Notations

Notation	Denotation
ADP	Atmospheric Downstream Plasma
BR	Bending radius
CCD	Charge Coupled Device
CMP	Chemical Mechanical Polishing
CMST	Center for Microsystems Technology
CTE	Coefficient of Thermal Expansion
DCE	Dry Chemical Etching
DI	De-ionized Water
DPW	Deep Proton Writing
EDM	Electric Discharge Machinig
EEL	Edge Emitting laser
EMI	ElectroMagnetic Discharge
EVPD	Edge Viewing PhotoDiode
FAOS	Flexible Artificial Optical Skin
FPC	Flexible Printed Circuit
FR4	Fiber Reinforced board material
FTDI	Future Technology Devices International
FTTH	Fiber to the Home
GaAs	Gallium(III)Arsenide
IC	Integrated Circuit
IPA	Isopropyl Alcohol
LAN	Large Area Network
LCD	Liquid Crystal Display
LDW	Laser Direct Write
MTM	Multitransverse mode lasers
NA	Numerical Aperture
OPAMP	Operational Amplifier
OPCB	Optical Printed Circuit Board
PBM	Polymer Chemistry and Biomaterials Group
PCB	Printed Circuit Board

PD	Photodiode
PEN	Polyethylene Naphthalate
PET	Polyethylene Terephthalate
PI	Polyimide
RCC	Resin Coated Copper
rh	Relative Humidity
RIE	Reactive Ion Etching
Rms	Root mean square
rpm	rounds per minute
SEM	Scanning Electron Microscope
SMA	Subminiature version A coaxial RF connector
SMD	Surface Mount Device
SMT	Surface Mount Technology
SOI	Silicon on Insulator
SU8	Negative Photoresist
TIA	TransImpedance Amplifier
TM	Trademark
TTV	Total Thickness Variation
USB	Universal Serial Bus
UTCP	Ultra Thin Chip Package
UV	Ultra Violet
VCSEL	Vertical Cavity Surface Emitting Laserdiode
WG	Waveguide
WYKO	Non-contact optical profilometer
YAG	Yttrium Aluminium Garnet

Chapter 1

Introduction

In the world of electronics, we not only see the trend of changing electrical interconnections into optical interconnections but we also see an expanding growth in the market of flexible substrates. The combination of mechanical flexibility and the presence of optical communications inside a foil presents a promising new technology platform which combines the advantages of both and enables a wide range of new applications.

1.1 Optical on-board interconnections

1.1.1 Introducing light into data communication

Light as a transmission medium for data communication has proven its success for many years. Driven by the increasing amount of phone calls in the middle 1960's, the optical fiber was developed. Dr. Donald B. Keck from Corning Inc. states [1]: "In the 30 years since our invention of low-loss fiber, more than 300 million km of optical fiber have been deployed worldwide". Optical fibers use the principle of total internal reflection of light within a core material surrounded by lower refractive index cladding material. The major advantages of this principle are the significantly lower propagation losses and the possibility to transport much higher bandwidths than electrical interconnects. Over long distances like intercontinental and intercity connections, the optical interconnects have thus been the obvious choice. A recent trend is the provision of optical fibers right upto the homes and businesses, called Fiber-to-the-Home (FTTH) which is yet employed for about 15 million users worldwide to insure access to the bandwidth-hungry services that are being developed today.

Also for shorter distance interconnections (rack-to-rack, board-to-board, Mul-

tiChipModules, on-board), the need for optics is rising, pushed by the ever increasing speed of computer chips. Copper tracks have always been relied on for this kind of communication, but due to the rising data-rates and their sensitivity to EMI (Electro Magnetic Interference), they soon could be unable to keep up. In fact, if Moore's law holds true and processing speed continues to double every 18 months, it is almost certain that a PC built in 2015 will require some form of internal optical data-bus to wire up its different chips. Moore's law however is reaching its turning point. The ever decreasing transistor footprint will saturize due to the reach of some critical physical limits. Advanced packaging techniques like 3D packages are believed to take over Moore's law and to keep pushing the increase of data speed. Over the next decade the datarates over interconnects inside a computer are expected to increase by several orders of magnitude - from around 1 GHz to 1 THz. This increase will require a shift in technologies from the electrical to the optical domain. Ian Young, director of Advanced Circuits and Technology integration at Intel's technology and manufacturing group states: "Maybe an electrical solution will stretch to 13-15 Gbit/s, but other factors will start to come into play, such as the cost and ease of manufacturing. We're targeting an optical solution at the 20 Gbit/s rate and upwards. We believe that optics could be playing a role in board-to-board links in as little as 2 years time, but that it will be least seven years before it is developed for chip-to-chip communication." [2].

Pushed by the above mentioned trends, a range of technologies, materials, know-how and components for on-board optical communication were developed and made available during the last decade. Several light guiding approaches were put forward, mainly divided in three categories: free space optics, discrete optical fibers and polymer waveguides. The state-of-the-art, advantages and disadvantages and the market possibilities of all these technologies were discussed and compared many times before. Therefore we will refer to [3, 4] for more background information. This PhD work will mainly focus on the extension of on-board optical interconnections towards flexible substrates. From all the light guiding approach possibilities, the obvious choice is the use of polymer optical waveguides. This is due to the versatile fabrication possibilities, the large variety in polymers and the availability of processing tools and know-how in the PCB fabrication market generally.

1.1.2 Pushing integration to its limits

The integration of optical waveguides and opto-electronic components inside a flexible foil introduces a complete new concept of flexibility into the on-board optical communications. In Section 1.1.1, we discussed the use and future market possibilities of light as transmission medium to counter the approaching physical limits of copper tracks. The bottlenecks of copper tracks due to increasing data

rates are however expected to rise up in first instance on high-end computers and later on on regular personal computers, both being applications which do not involve flexible substrates, but rigid cards, motherboards, racks, ... Using optical interconnections in flexible foils has many other uses and advantages than rather the tackling of the increasing data rates problems. These applications areas will be stated and discussed in Section 1.3.

The research on the embedding of all optical and opto-electrical features inside a 150 μm thin foil introduces the concept of mechanical flexibility but also a significant level of system integration and compactness beyond the state-of-the-art to the best of our knowledge. All VCSEL's, photodiodes, VCSEL drivers, TIA's, IC's, waveguides, optical coupling structures, galvanic interconnects and heat sink features will be embedded in a total stack of only 150 μm thickness. The great benefit of this miniaturization technology is the drastic reduction of footprint and volume of an active optical waveguide link, which could make the optical waveguide link as chip-to-chip data connection much more attractive.

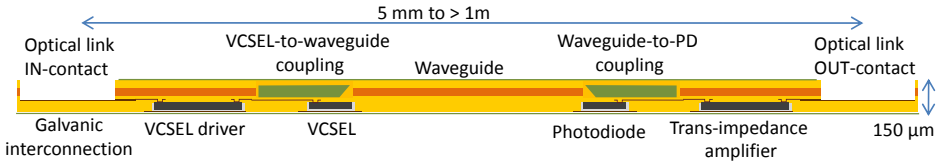

Figure 1.1: Overview on the cross-section of the different embedded components inside the active optical waveguide foil.

The foil that will be developed and presented within this PhD research will be completely flat and will only have an electrical interface to the outer world. All features needed for the optical data transmission, consisting of consecutively VCSEL driving signal conditioning, electrical-to-optical conversion, optical-to-electrical conversion and signal amplification, will be inside the foil, virtually invisible to the outer world. This means that the total link foil will act as a standard electrical interconnection, but with a much higher bandwidth. The high level of integration also provides the smallest possible intermediate transmission lengths. The length of the optical path from VCSEL to waveguide and from waveguide to photodiode will be minimized as well as the electrical interconnections from the foil contact pads to the embedded electronics contact pads. The latter is a must for the realization of high throughput data links, since there is no use of applying an optical link when the electrical path to the optical link remains too long. Figure 1.1 shows an overview on the cross-section of the different embedded components inside the foil.

The acceptance of optical waveguides in the market of the classic on-board

electronics is evolving very slowly since there are still a lot of drastic adjustments to be done to nowadays electronic components, to board lay-outs and supply chain tools. Grouping every single feature of the optical link inside a very thin, compact foil can reduce these adjustments to almost zero. The optical link foil can be mounted on top of the board, can be laminated in between multilayer PCB's, can be positioned over other SMD components or any irregular surfaces since it is completely flexible. Alignment of the optical link on the board is a standard PCB process since no optical alignment tolerances need to be taken into account, the foil has only an electrical interface.

Compatibility of the optical link with PCB manufacturing will be proven in this work. This means that the optical link survives the reliability tests for standard electronics and is able to withstand any PCB manufacturing process temperature and process chemicals. Because of the flexibility of the optical link, no CTE mismatch concerns between board substrate and the foil will occur. Moreover, every dimensional change in the board substrate due to temperature or stresses will have no influence on the foil, again because of its flexibility.

The optical link foil brings a solution where an extremely high bandwidth is demanded. The very small thickness of the foil (150 μm) allows for multilayer optical links stacking without any additional technological concerns. Galvanic interconnection of the different layers is easy because the foil is thin enough for the use of laser ablated via's for this purpose. This way the footprint of the interconnection can be reduced to a minimum. Moreover, the footprint can be reduced to zero, since both ends of the optical interconnection foil can be mounted on top of the transmitter and receiver chip, while the waveguide part of the foil is up in the air, as a kind of "arc" between receiver and transmitter.

All above mentioned advantages of the flexible optical link foil are referred to as an additional value to existing rigid electronic and opto-electronic boards. Most of these advantages are a reflection of the high degree of integration which is achieved in this work. To frame this new technology in the present state-of-the-art, we will give an overview of the different levels of integration of opto-electronics and waveguides onto rigid opto-electronic boards as they were presented in publications over the past few years. Figure 1.2 and Figure 1.3 summarize the reported opto-electronic mounting principle schemes:

Vertical light confinement between opto-electronics and waveguides

Figure 1.2(a): (Source: a1: [5]; a2: [6]; a3: [7]; a4: [8])

An approach which has been put forward by different research groups is the lamination of optical layers in between multilayer PCB's. This way they do not

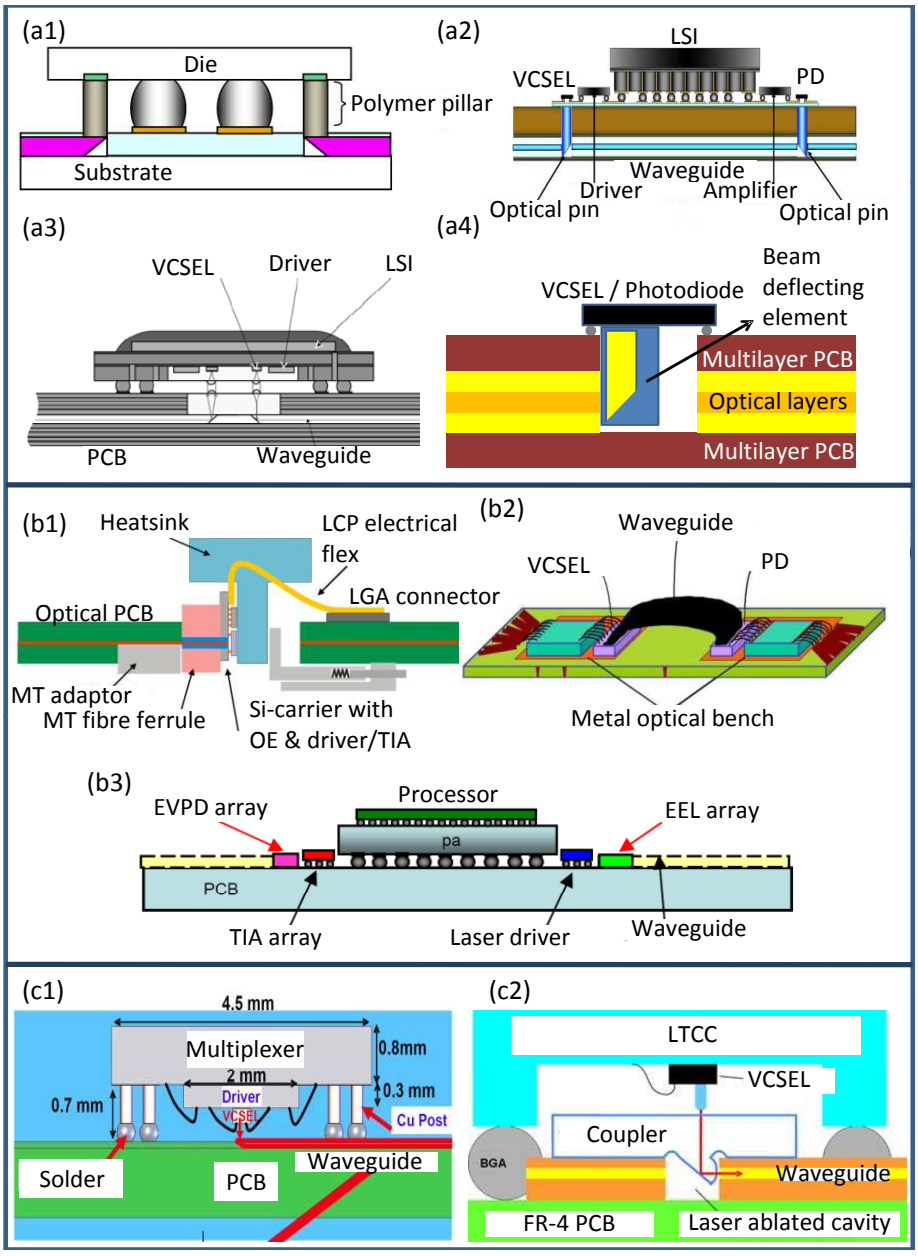

Figure 1.2: State-of-the-art opto-electronic mounting principle schemes (Part 1).

interfere with the component assembly on the top and bottom of the board. The opto-electronic components like VCSEL's and PD's are then mounted on top of the surface with solder techniques. Another approach is the stacking of transmitter chip, VCSEL driver and VCSEL (or on the other side: receiver chip, TIA and PD) on top of each other in one single BGA package and mount this on top of the substrate surface. In this kind of set-up, the actual distance between the VCSEL/PD and the waveguide becomes too large. To prevent that the light diverges during the propagation over this distance, several techniques were put forward to confine the light in this vertical part of the light pad: intermediate waveguides like polymer pillars (a1)[5], 45^o finished optical fibers (a2)[6, 9, 10] and other beam deflecting elements (a4)[8]. The use of lens systems instead of intermediate waveguides as in (a3) can also couple the light into the waveguide with relative high efficiency. The latter technique has the additional advantage that it eases the alignment tolerance of the mounted SMT package: this kind of interface provides an alignment tolerance of ± 50 μm , which is large enough for use with the SMT process.

In-plane coupling approaches

Figure 1.2(b): (Source: b1: [11]; b2: [12]; b3: [13])

VCSEL's as light source are considered to be the most economical solution and are consequently the most widely adopted in parallel optical interconnections. However, the combination of vertical emitting components and horizontally positioned waveguides demands for 45^o beam deflection with micro-mirrors. These incorporate a lot of extra optical losses in the lightpath. Several coupling techniques were reported to eliminate this loss by using butt-coupling. In this technique, the light beam is emitting in the same direction of the waveguide, eliminating the need for mirrors. In (b1)[11, 14], a cavity is fabricated inside the polymer layer, allowing the VCSEL's to be mounted vertically as shown in the Figure. In (b2)[12], the VCSEL's and PD's are mounted in the normal way, but the waveguides are mounted vertically on top of the VCSEL's. Due to the flexibility of the waveguides, the light can be guided in bended directions. Finally in (b3)[13, 15], Edge Emitting Lasers (EEL) and Edge Viewing Photodiodes (EVPD) are used as an alternative to standard VCSEL's/PD's.

Vertical proximity approach

Figure 1.2(c): (Source: c1: [16]; c2: [17])

To minimize the distance between the opto-electronics and the waveguides, dedicated BGA package approaches were presented. One consists of using Cu

posts to elevate the transceiver chip in such a way that the VCSEL is positioned very close to the substrate surface (c1)[16]. A second method consists of mounting the BGA balls in places where the optical layers are removed, so the BGA package is lowered (c2)[17, 18, 19].

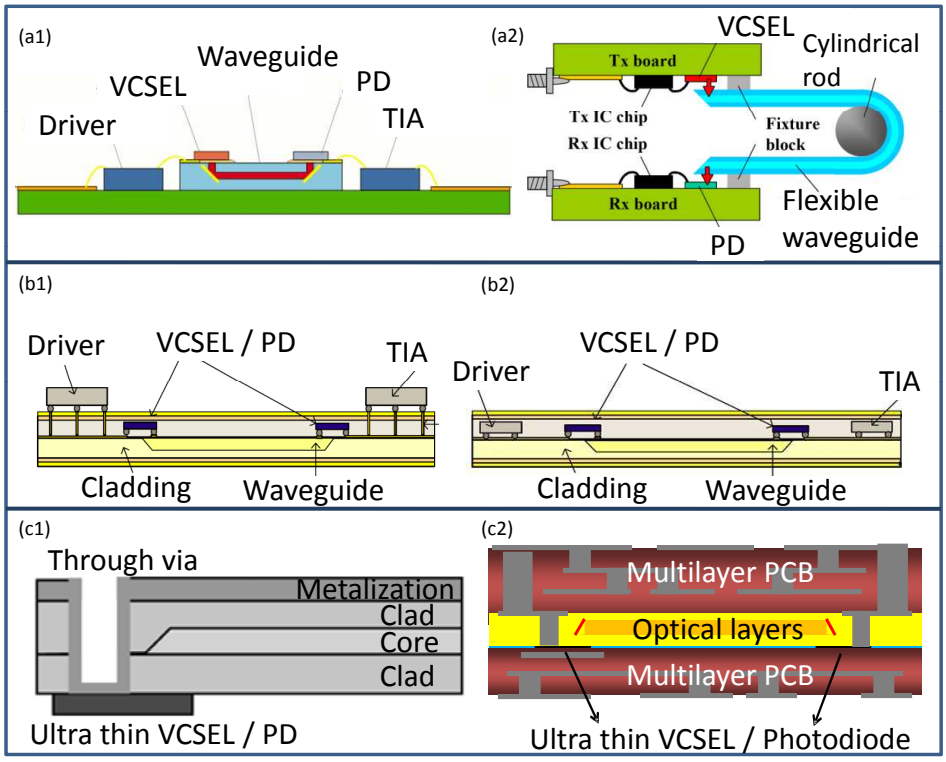

Figure 1.3: State-of-the-art opto-electronic mounting principle schemes (Part 2).

Separate waveguide PCB approach

Figure 1.3(a): (Source: a1: [20]; a2: [21])

As an alternative to the laminated waveguide layer, they can be fabricated on an external substrate and then mounted on top of the mother substrate. In (a1)[20], the opto-electronics are mounted on top of the waveguide stack and wire bonded to the mother substrate, while in (a2) [21, 22], they are mounted on the mother board.

Embedding of opto-electronics by RCC lamination

Figure 1.3(b): (Source: b1: [23]; b2: [24])

After mounting of the opto-electronics on the optical layers, they are embedded by the lamination of RCC layers. In first reports (b1)[23, 25, 26, 27], the driving electronics were assembled on the top of the RCC layer, while in later reports (b2)[24, 28], they were also embedded inside the RCC layer to lower the surface footprint even more.

Embedding of ultra-thin opto-electronics by standard lamination

Figure 1.3(c): (Source: c1,c2: [29])

Another approach on the embedding of the opto-electronics is presented in (c1)[29, 30, 31, 32, 33, 34, 35, 36, 37, 38]. The VCSEL's and PD's are thinned down chemically (with etch stop layer) to a final thickness of only 10 μm and mounted onto the waveguide foil. Due to the thinness of the devices, they do not cause planarization problems during the lamination process of the waveguide layers in between multilayer PCB's as shown in (c2).

1.2 Flexible substrates

Electrical circuits on flexible substrates are not new to electronics manufacturing. The technology actually has a surprisingly long and rich history. Patents issued at the beginning of the 20th century show clear evidence that early researchers were thinking of how flat conductors sandwiched between layers of insulating material could ease the layout of certain, primitive types of electrical circuits in early telephony switching applications [39]. Growth and proliferation of flex circuit technology from that point was slow initially, but it has been accelerating ever since. Today, flexible circuits are used in nearly every imaginable type of electrical and electronic product. Over the last several years, flexible circuits have remained one of the fastest growing of all interconnection-product market segments. According to Joseph Fjelstad [39] international authority, author, columnist, lecturer and innovator with more than 150 issued and pending US patents in this field, it is easy to forecast that flexible circuits will continue to attract increasing numbers of both users and manufacturers.

The report from BPA Consulting Limited [40] - one of the most accurate forecasters of IC packaging and materials - on "Worldwide Technology and Market Trends for Flex and Flex Rigid Circuits 2008-2013" states that the world market has doubled from just under $4 billion to over $8 billion in the 5-year period from

2002 to 2007. Figure 1.4 shows the evolution of the flex and flex-rigid market from 1984 to 2008 based on several reports from BPA Consulting. The share of flex circuits within the total PCB market has increased from 4.4% in 1984 to 19.7% in 2008, with an expectation towards 25% in the coming 5 years. The key growth areas for flex are the mobile phones , display interconnects, digital cameras and other small portable equipment.

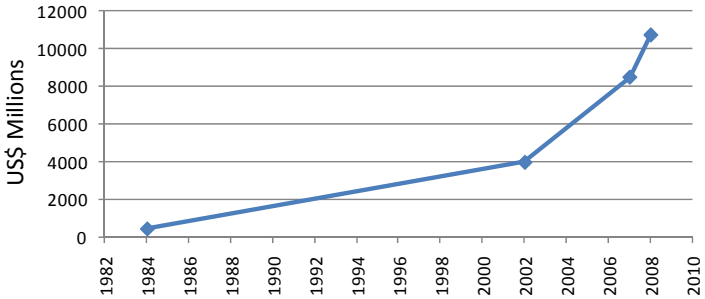

Figure 1.4: The evolution of the worldwide flex and flex-rigid market from 1984 to 2008 based on several reports from BPA Consulting.

The drivers for the use and need of flexible circuits are versatile. The possibility of dynamic flexing makes them the obvious choice by the lacking of viable alternatives. This is however a small portion of the advantages of flexibility. A flexible substrate is the thinnest dielectric substrate available today, which results in a significant reduction in package size, which is even more enhanced by the formability of the substrate. Since flexible substrates have a very light weight and do not employ reinforcements (like screws, spacers, etc.) compared to rigid substrates, there exists a large benefit in total system weight. This is why they are so popular in aerospace applications over the years, but it is also an attractive feature in portable electronics, which now regularly compete on size and weight. Assembly time, cost and error frequency can also be reduced by changing to flexible substrates, especially for point-to-point interconnections. Concerning system reliability: when an electronic package of any type fails, it most typically fails at some point of interconnection. Flex circuits reduce the number of levels of interconnection required within an electronic package or assembly and thus improve the reliability.
Moreover, flexible substrates enable roll-to roll or reel-to-reel techniques. This adds a drastic improvement on fabrication speed, cost and reproducibility compared to sheet-to-sheet or board-to-board techniques.

1.3 Flexible optical foil at work: market and application opportunities

In Section 1.1.2, the flexible optical link foil developed in this PhD work is referred to as an added value to optical communications on existing **rigid** electronic and opto-electronic boards.
This section will try to map the market and application opportunities for the flexible active optical foil when used as a **flexible** entity. The areas of application are very diverse:

1.3.1 Optical wiring

It needs no explanation that wiring of different systems and subsystems is preferable flexible. For optical wiring, glass and POF fibers are widely accepted and applied. Their minimum bending radius and large diameter size however can result in quite bulky solutions when hundreds to thousands of fibers come into play. A flexible waveguide foil offers a highly parallel solution for this issue. Main applications can be found in the optical interconnection on board, rack to rack, board to board and even chip to chip. The flexibility of the waveguides enables compact 180 degrees optical coupling of racks and boards, 90 degrees coupling of mother with daughter boards, hinge-like optical interconnects in mobile phone hinges and on board bended optical connections. Figure 1.5 gives an overview.

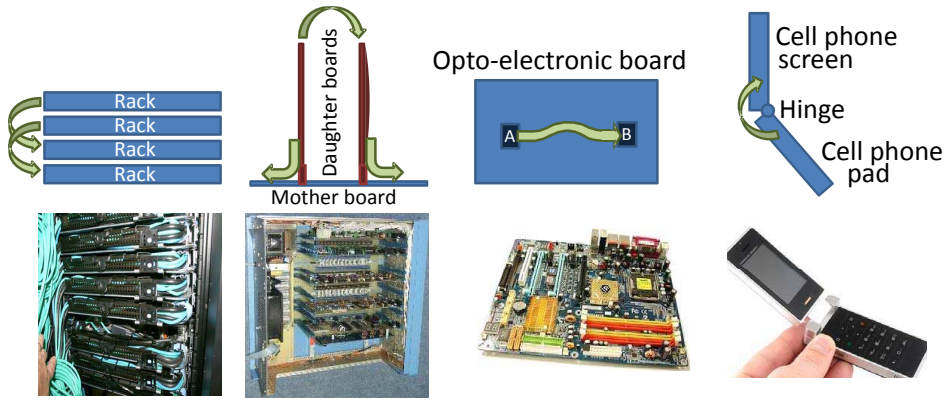

Figure 1.5: Overview of the current application market possibilities for the flexible optical waveguide foil.

The waveguide foil can be used purely as a transmission medium but can also accommodate passive functionalities by implementing splitter and multiplexer structures applied on the waveguides. This results in optical re-routing applica-

tions in complex opto-electronic systems. The use of polymer waveguide foils can also eliminate the cost of terminating and connecting of separate fibers and improves the fragility and reliability of the wiring significantly. The worldwide research, reports and applications of flexible optical waveguide films has been growing exponentially in the past years for optical wiring purposes. Figure 1.6 shows the amount of patents on flexible optical waveguides from 1984 to March 2009 and the amount of patents on materials for flexible optical waveguides.

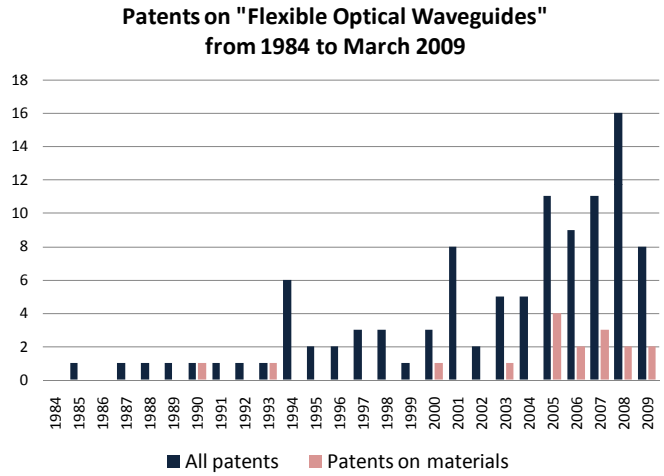

Figure 1.6: Amount of filed and accepted patents on flexible optical waveguides from 1984 to March 2009 and the amount of patents on materials for flexible optical waveguides.

1.3.2 Optical sensor systems

Although the most important application of optical fibers and waveguides is in the field of transmission of information, their capability of sensing various physical parameters and generating information are also finding widespread use. Their use offers the same advantages as in the field of communication: lower cost, smaller size, more accuracy, greater flexibility, and greater reliability. As compared to conventional electrical sensors, optical sensors are immune to external electromagnetic interference and can be used in hazardous and explosive environments. A very important attribute is the possibility of having distributed or quasi-distributed sensing geometries, which would otherwise be too expensive or complicated using conventional sensors. With optical sensors it is possible to measure pressure, temperature, electric current, rotation, strain, chemical and biological parameters with greater precision and speed. These advantages are leading to increased integration of such sensors in civil structures such as bridges

and tunnels, process industries, medical instruments, aircraft, missiles, and even cars.
The optical sensing methodologies are versatile: Intrinsic/extrinsic sensors, transmission/reflection sensors, intensity/interferometric sensors, point/distributed sensors, etc. Trying to unravel all the opportunities for the active flexible optical waveguide foil in all these methodologies, for all the application fields would bring us much too far. Therefore we will describe in general lines what the active optical foil could bring as additional value to the existing optical sensing technologies.

Whatever optical sensing technique is used, one will always need a light source, a light detector and signal analyzing electronics. In many cases it is preferable to bring source and detector as close to the measurement area as possible. This is however not always possible since standard electronics and opto-electronics packages together with coupling structures are quite bulky. Moreover if for example the measurement area is a fluidic substance, the electronics should be kept out of it. The embedding technology presented in this PhD work eliminates this problem, since the electronics and opto-electronics can be embedded very close to the measuring area, so that they can be entered inside the measured medium without the need for additional packaging.

An often stated requirement for sensing is compactness. The sensing locations of interest are dedicated and often very small and difficult to reach. For many applications, the highest level of compactness would be preferable. The active optical foil presented in this research answers to this demand as it is a foil of only 150 μm thin and can be laser-cut to the desired shape. This means that the actual sensing element will only be as large as the bare opto-electronics needed for light emitting and detecting, and as long as the optical waveguide path needs to be. In case of distributed sensing instead of one-point sensing, the resolution of the sensing points is often dependent on the size of the sensing elements with electronics included. In those cases, we can again say that "smaller = better".

The majority of sensors applied today in the wide application market are not really part of a functional system, but are merely monitoring devices, which measure in real time if certain variables are not exceeding their requirement values. They only play a role when something actually goes wrong in the monitored system. Therefore the sensor should be as unobtrusive to the system as possible. This implies that the sensor should be as thin as possible. Also flexibility is of importance as detecting surfaces and the way to reach these surfaces is rarely completely flat. Some specialized systems need hundreds to thousands of sensor points, meaning that the manual placement, routing and connectorization can become an issue in terms of reliability, human errors and routing complexity. The use of completely flexible sensors can ease these processes and improve the

reliability.

1.3.3 Portable / Wearable applications

As depicted in Section 1.2, the main driver of the current boom in flexible electronics comes from the field of portable applications. The demand for mobile phones has increased from 400 million to 600 million in only three years from 2001 to 2004 [40]. Not only the amount but also the diversity and the performance of portable devices is expanding immensely. Remember your cell phone 10 years ago and look at it today. No need to explain that an ever increasing complexity in an even smaller device volume needs some innovative technologies. This is why it is no coincidence that the market of mobile cell phones are believed to be the first industry to actually bring optical waveguide communication into production [41]. Omron Corporation reported a highly flexible purely optical interconnection through the hinge of a cell phone, eliminating any electrical interconnection through the hinge [42].

Not only the hinge within a cell phone creates flexibility demands but also sliding opening mechanisms and interconnects to the display module, camera module and hard drives. The increasing pixel count required for improved display consequently requires an increase in the routing density. This has pushed the shift to double sided electrical flex interconnects and later on in multilayer flexes [43]. The use of optical waveguides in this market segment can reduce the interconnection circuit size and thickness significantly.

In Section 1.1 we discussed the future implementation of active optical interconnections in on-board technologies and in Section 1.2 the emerging trend towards flexible interconnections in portable applications. At some point we can expect these two trends to meet each other, where a need for flexible optical interconnection will be created. The developments presented in this PhD research bring a solution to these future demands in portable devices pushed by a continuous drive to reduce size and mass while performance increases.

Integrating electronics into clothing is a major new concept, which opens up a whole array of multi-functional, wearable electro-textiles for sensing/monitoring body functions, delivering communication facilities, data transfer, individual environment control, and many other applications. With revolutionary advancements in many fields of science and electronics the possibilities offered by wearable technologies are very diverse and widespread. Companies such as Body Media [44], Sensatex [45], Textronics [46] and Vivometrics [47], are going a long way in addressing the need for more consistent and remote monitoring of individuals including elderly care, chronic disease management, and others. These solutions are just beginning to transition from the development phase into

commercialization. The opportunities of flexible waveguide optical interconnections in this application segment are comparable to those in portable applications, discussed above.

1.3.4 Harsh environments

Automotive

The rising demand for safety, comfort, multimedia, infotainment and fuel-saving applications in automobiles pushes the integration of photonic-based technologies in the automotive industry. Automobiles are increasingly employing photonics for lighting, displays, sensors, and communications systems due to their superior behavior in terms of data rates, bandwidth, reliability, and robustness.

For recently introduced infotainment systems with high-speed audio and video transmission at data rates of more than a few megabits per second, shielded electrical cables or complex electrical drivers are required to avoid electromagnetic interference (EMI) within the cable harness of the car. In contrast, fiber-optic data links are insensitive to EMI and are a cost-efficient alternative to shielded electrical wires. Optical interconnections networks are nowadays already present in high-end cars, where they also introduce a considerable weight reduction, and thus lower fuel consumption.

Moreover modern cars contain hundreds to thousands of sensors. Fiber optic sensors robustness and resistance to harsh environments have made them well suited for automotive applications. The major new application areas of optical sensors in cars are driver assistance systems and traffic monitoring systems.

Parallel with the upcoming trend of optical networks in automobiles, there is also a trend towards MacroFPC's [48]. These are very large (car size) flexible electrical printed circuit boards which replace the classic round cable harness and results in a harness weight reduction upto 55%. The use of such macroFPC's also reduces the assembly time considerably and enables integration of electronic components, eliminating the need for connectors.

One can expect that if both trends will continue, the future car harnesses could be one day consisting of flexible optical waveguides. Integration and coupling of light sources, detectors and signal conditioning electronics, as will be presented in this work can find their application within this area of technology.

Medical devices

Flexible electronics are widely used within hearing aids, pacemakers, defibrillators and large imaging equipment. Reasons of reliability and compactness were the main drivers for the transition from rigid to flexible substrates. The role of optical communication in this field is rather limited. However, the use of optical sensors has become prominent. This is the area of interest concerning the work presented here (see Section 1.3.2).

Avionics

A simple, reliable, low-power and lightweight network that is free from the effects of electromagnetic interference and capable of supporting the broadband communications needs of future onboard digital avionics systems cannot be easily implemented using existing coaxial cable-based systems. Fiber-optical communication systems can meet all these challenges of modern avionics applications in an efficient, cost-effective manner. Same remarks towards flexible waveguide harnesses can be made as in the automotive industry.

Space

The use of optical interconnections can introduce a considerable decrease in fuel consumption and associated cost reduction because of the lower weight.

1.4 Research context

The research which formed the base of this dissertation was carried out within the framework of following projects:

- NEMO (Network of Excellence on Micro-Optics) [49]
  European IST-Project, Framework 6, 2nd call
  Workpackage on Micro-Optics for PCB and MCM-level interconnects
  Starting date : September 1, 2004
  Finishing date : August 31, 2008
  Project coordinator : Prof. Dr. Ir. Hugo Thienpont, VUB Vrije Universiteit Brussel, Pleinlaan 2, B-1050 Brussels, Belgium

  NEMO's mission statement is to set up a world force on micro-optics research and technology.

- FAOS (Flexible Artificial Optical Skin) [50]
  SBO project, funded by the Flemisch Institute for the Promotion of Innova-

tion by Science and Technology (IWT [51])
Worpackage 2: Integration technologies
Starting date : January 1, 2007
Finishing date : December 31, 2010
Project coordinator : Prof. Dr. Ir. Peter Van Daele, IMEC - Ghent University / CMST Microsystems, Technologiepark 914A, B-9052 Zwijnaarde, Belgium

The FAOS-project aims at developing a flexible substrate or foil in which the sensing elements can be integrated and in which also the light sources, detectors and electronic circuitry are embedded or integrated on compact signal processing boards. This artificial and flexible optical sensing foil can then be applied to irregular surfaces (e.g. for distributed sensing applications), on moveable surfaces (e.g. in robotics) or can folded into compact modules (for portable devices, automotive, etc).

- PHOSFOS (Photonic skins for Optical Sensing) [52]
  European ICT-Project, Framework 7
  Workpackage 4: Integration
  Starting date : April 1, 2008
  Finishing date : March 31, 2011
  Project coordinator : Prof. Dr. Ir. Francis Berghmans, VUB Vrije Universiteit Brussel Pleinlaan 2, B-1050 Brussels, Belgium

  The PHOSFOS-project aims at developing a flexible and stretchable foil that integrates optical sensing elements and that if necessary, appropriate and relevant to the application, can include optical and electrical powering as well as onboard signal processing and wireless communications. This skin can be wrapped around, embedded in, attached and anchored to irregularly shaped and/or moving objects or bodies and will allow quasi-distributed sensing of mechanical quantities such as deformation, pressure, stress or strain.

1.5 Research dissemination

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Chapter 2

Flexible optical materials

Taking on-board optical waveguides to a next generation by bringing flexibility into the game, brings on some additional technological challenges. The optical waveguide material needs to prove excellent bending behavior and endurance. The existing optical material market is rapidly expanding, though commercial availability still is a major drawback. This chapter gives an overview of the material requirements, the existing materials, the used materials in this thesis and material modifications.

2.1 Introduction: The quest for material

Materials for flexible optical interconnects must fit a load of requirements. Two obvious requirements are however prominent: flexibility and optical transparency. At the start of this research, such materials were only in a preliminary research status and now, 4 years later, they are much more developed but still not commercial available or extremely expensive. This chapter gives an overview of the materials on the market and the worldwide research progress on flexible optical materials, reported in scientific publications.

To cope with the lack of flexibility in available materials and the non-availability of flexible materials, development of new formulas and compounds has started. Within the IWT funded FAOS project [1], close cooperation with the PBM Group (Polymer Chemistry and Biomaterials Group) of the Ghent University was set-up to take on this task. This chapter presents the results and discussions.

2.2 Material requirements

The requirements for a material in a demanding application as flexible optical interconnections are numerous. To get a better overview, we will group them into three separate categories: optical , mechanical and PCB-manufacturing related requirements.

Optical requirements

When using optical waveguides as a transport medium for light, the waveguide material needs to fulfill some demands in the field of transparency and refractive index since it is a part of the light path:

- **Low optical bulk loss**: The material must show low optical losses at a wavelength of 850 nm for datacom applications or 1.3 and 1.55 μm for telecommunication applications. The use of waveguides in optical sensing applications can demand low losses at other wavelengths or even large wavelength ranges.
- **Smooth surfaces**: When features like waveguides, lenses or micro-mirrors are fabricated in the material, they must have a smooth surface, since any large scale irregularity ($\geq$ wavelength /10) on the surface will result in additional scattering losses.
- **Refractive index tunability:** When bending a waveguide, the wave conditions for total internal reflection are changed and the acceptance angle of the waveguide changes, which will cause additional bending losses. When applying very small bending radii, this bending loss principle can be compensated for by raising the refractive index variation between the waveguide core material and the cladding material. Therefore it is preferable that the material is tunable in its refractive index.

Mechanical requirements

The mechanical requirements reflect mostly on the flexibility of the material. The trivial aspect flexibility is a macroscopic characteristic which is determined by the material thickness and Young's modulus. The lower the Young Modulus and the thinner the material, the higher the flexibility will be. To quantify this mechanical property and define the requirements, following parameters can be investigated:

- **Minimum bending radius :** All materials can be bent to a certain level as long as the layer thickness is small enough. The minimum bending radius at which they can be bended without deformation or fatal damage must

however be as small as possible. Materials with a minimum bending radius of 5 mm can be called flexible, but for excellent bendability, a minimum bending radius of about 2 mm is demanded.

- **Bending durability :** In dynamic applications such as a hinge-like structure, the material has to be bended for over 1000 times. For reliability purposes, the materials must be able to withstand over 100000 bending cycles without any change in its original characteristics.

- **Helical bending :** Is some applications the flexible waveguides need to be helically bent. Durable behavior in this sort of deformation must be showed.

Processing requirements

The world wide PCB manufacturing combines a lot of established processes, tools and requirements. If we want the acceptance of a new on-board technology to take place within a reasonable time scale, we need to be sure the technology is compatible with the existing PCB technologies. This compatibility starts with the compatibility of the materials:

- **Deposition :** The formation of a material layer is done by applying the material uniformly over the complete substrate. Many techniques like spin-coating, doctor blading, screen printing, dip coating, curtain coating, dry coatings, etc.. are available, but each deposition technique has its own requirements for the material. With most of the techniques however, only the viscosity of the material plays a role.

- **Process compatibility :** A dozen waveguide fabrication processes have been reported in the past (See Section 3.2 Chapter 3). When a preferred process is chosen, the optical material should be compatible with that process, show low surface roughness and perfect reproducibility.

- **Good adhesion :** The optical material layers should show good adhesion to the rigid PCB board as well as to each other since a waveguide stack consists of different cladding and core layers. Delamination is a frequent reliability problem when stacking different types of material layers.

- **Chemical resistance :** Optical polymer waveguides are almost never used as stand-alone passive light guiding components, but are integrated with opto-electronics circuitry and components. Therefore the optical materials need to be resistant to the chemicals used in standard PCB fabrication process (acetone, isopropanol, water, etchants,...).

- **Heat resistance :** The polymer material has to withstand the high temperature and pressure that occur during a lamination step (typically 180^{o}C) and solder reflow step (typically 240^{o}C, but this can be even higher in case lead-free solder is used).
- **Reliability requirements :** Electronic designers can count on a very well settled standard for reliability testing, while opto-electronics still lack on this matter. Therefore the reliability tests of electronics are often performed on optical structures too. Main testing comprises fast temperature changes, humidity, corrosion, long term heat stability, etc..
- **Cost :** As for all applications, the cost is one of the major factors which determines the speed of introduction of the application into the market. For high-end low throughput applications, this constraints is however less prominent.

Polyimide sandwiching requirements

In Chapter 4, a method is discussed to improve the flexibility of materials which do not fulfill the mechanical requirements. The waveguide stack is sandwiched in between two spin-coated Polyimide layers. This process implies a few additional requirements:

- **PI adhesion :** Since the internal forces inside the material during bending has to be taken up by the outer PI layers, the adhesion between the PI layers and the waveguide layers must be optimal.
- **Coefficient of thermal expansion (CTE) :** PI layers and the optical polymer must have a similar CTE to decrease the chance of delamination during thermal aging tests.
- **Heat resistance :** PI has a high curing temperature, so the sandwiched waveguide layers must be able to withstand these temperatures (210^{o}C-350^{o}C, depending on the type of PI).

2.3 State-of-the-art waveguide materials

Reports on the realization of optical waveguides of the last two decades comprise a large variety of material families. In what follows, we try to give an overview on all the materials by using the requirement groups of Section 2.2 as benchmarks. Figure 2.1 shows the Venn diagram we will use for the further material overview in this Section.

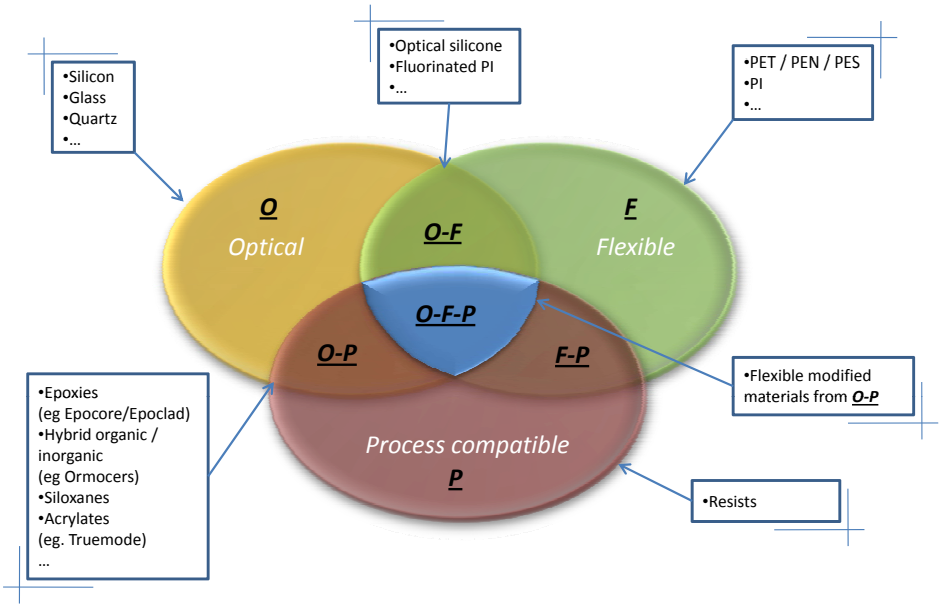


Figure 2.1: Venn diagram of the material market, bench marked according to the proposed material requirements.

A complete listing of all reported flexible waveguides to the best of our knowledge is shown in Table 2.5. The table states the used materials, providers, fabrication techniques and optical characteristics.

2.3.1 Group O: Optical materials

This group consists of mainly inorganic optical materials. Inorganic materials such as silica, silicon oxynitride, lithium niobate, indium phosphide and gallium arsenide are often employed in the fabrication of modern integrated optics as these materials have the advantages of thermal stability, chemical inertness, transparency and low birefringence. However, they also have the disadvantage of a high production cost compared with other materials [2].

2.3.2 Group P: Process compatible materials

A lot of high reliable, thermal stable and diversely patternable polymers is available nowadays for PCB applications. Polymers are attractive materials due to their versatility, light weight, low cost and ease of modification [3]. However,

most polymers contain hydrocarbon groups which results in high optical losses due to the second harmonic vibrational absorption of CH bonds [4], particularly in the near-infrared region. Polymeric materials also experience a large volume shrinkage induced by curing as well as internal stress during many fabrication processes, resulting in an increase in the level of optical loss at key communication wavelengths [4].

2.3.3 Group F: Flexible materials

Most common flexible substrates are PEN, PET and PES for cheap applications and PI for high performance applications. The PEN, PET and PES materials however do not fulfill the process compatibility requirements, PI is difficult and expensive to pattern (see Section 2.3.4) and they all show high optical propagation losses.

2.3.4 Group O-F: Optical, flexible materials

Silicones

A special group of polysiloxanes is known as "silicones". Organosilicon compounds have been investigated since the end of the 19th century and have been developed leading to materials which have different properties and features from common carbon-based organic compound. Silicone is composed of continuous siloxane bonds (-Si-O-Si) with alkyl and phenyl groups. The main chain Si-O bond length is longer than the C-C bond length and the rotation energy of a Si-O bond is smaller than a C-C bond. Therefore Si-O bonds can be moved easily and the Si-O based compounds show very good flexible behavior. Additionally Si-O bonds are more stable than C-C bonds since the bond energy of the Si-O bond is higher than that of C-C bonds. Thus the Si-O based compounds have high thermal stability. Generally, most flexible materials do not show good heat resistance but silicones do show both flexibility and heat resistance.
With these characteristics, silicones are widely applied in many research fields and can be expected to play a key role in flexible optical communication systems but processability is a major downside. Patterning of waveguide-, coupling-, and alignment- structures in silicones can be done by fast replication methods like embossing, casting, moulding, etc. But any other patterning technique still shows major issues. Photosensitive silicones are reported but this technology is still immature with poor patterning quality. Other patterning techniques like laser ablation, wet etching and direct writing are impossible. Silicones are also often sticky and in cured status still very soft which makes the handling and processing very difficult. One last drawback is the poor adhesion of silicones to the main substrate materials and to metallization layers. The poor adhesion behav-

ior of silicones would cause a lot of problems when embedding actives, applying metallization layers, etc. in the rest of this research.

Fluorinated PI

Polyimide is the dominant material in the flexible circuits industry because of its numerous advantages including excellent flexibility at all temperatures, good dielectrical properties, excellent chemical resistance, very good tear resistance and a high glass transition temperature [5].
For optical waveguide application, the conventional polyimides are not the best candidates. Polyimides are polymers that usually consist of aromatic rings coupled by imide linkages that are linkages in which two carbonyl (CO) groups are attached to the same nitrogen atom. They are anisotropic and also tend to be highly colored due to intramolecular charge transfer complexes that form between the electron rich diamine and electron deficient dianhydride. These properties result in high optical absorption and scattering losses. Recent investigations to lower loss polyimides by adding fluorine in the system resulted in low loss fluorinated PI . One example of this Polyimide is provided by Amoco Chemicals [6].

The fabrication of waveguides in Fluorinated Polyimide have been reported using photolithography [7], reactive ion etching (RIE) [8] and moulding [9]. The latter claim to be the only one realizing waveguides in Polyimide using mass production replication techniques. Replication techniques are promising due to their low cost, but are generally limited to thermoplastic polymers with thermal stability lower than 200^{o}C.

Flexible organic semiconductors

Organic Light Emitting Diodes (OLED) and Photodiodes (OPD) have served a range of applications in the past decennium. In [10], the theoretical background of this technology is summarized. Development of flexible organic semiconductors for this purpose resulted in a range of flexible light emitting, light detecting and light amplifying materials. The knowledge about the use of these materials for passive waveguides is however limited and the materials are quite expensive. Therefore we will not focus on this group of materials in the rest of the research.

2.3.5 Group O-P: Optical, Process compatible materials

This Group is probably the most developed and diverse group of materials in the optical waveguide industry. The fabrication of optical waveguides on standard PCB boards is widely established, resulting in a lot of optical PCB compatible

materials, developed by many different providers. There is however still no leading material on the market at present [11]. In [12] you will found a detailed description of the world market of rigid optical waveguide materials in 2006.

The materials in this Group are mainly obtained by modifying polymers from Group P (Process Compatible materials) or combining formulations from Group O (Optical materials) and Group P, the latter resulting in inorganic / organic materials. In what follows, we will shortly describe both strategies and give more detailed information on four materials within this Group, which were used manifold within this PhD work.

Modified polymers

Polymers from Group P (Process Compatible materials) contain hydrocarbon groups which results in high optical losses due to the second harmonic vibrational absorption of CH bonds [4], particularly in the near-infrared region. One strategy to reduce these losses is to shift the associated vibrational absorption towards longer wavelengths by replacing hydrogen with heavier atoms such as halogens, particularly chlorine or fluorine [13]. Introducing fluorine in the aromatic systems provides an efficient approach without scarifying the thermal properties. Polymers such as deuterated or halogenated polyacrylates, fluorinated polyimides, perfluorocyclobutane ether polymers and perfluorovinyl ether polymers have been thoroughly investigated in past years. A number of these specialty optical polymers have been commercialized. The high cost of producing these compounds however limits their extensive use in photonics. Perfluorinated polymers also have poor adhesion to many substrates due to its low surface energies and inert nature.

Inorganic / organic materials

In order to achieve material properties superior to single organic or inorganic components, various types- of composite material in which two different phases with complementary physical properties are combined have been reported. Unlike classical approaches to produce macroscopic composite materials simply by mixing inorganic materials with organic compounds, they are prepared by sol-gel processing. Using this method, an organic-inorganic networklike structure is formed by crosslinking through a polycondensation reaction between inorganic precursors and organic compounds. This method avoids high volume shrinkage during further treatment. The non-hydrolytic sol-gel synthesis can be condensed well from the resin preparation stage, so there can be little further inorganic condensation reaction during curing steps. Thus, the shrinkage of cured samples is low enough to be applied to a micro-moulding process, during UV and thermal

curing steps (about 2.5 % volume contraction measured by Archimedes method [14]).
The combination of organic and inorganic building blocks enables precise tailoring of the optical properties of the materials (e.g. optical loss, birefringence, refractive index, and thermooptic coefficient) and the mechanical properties(e.g. flexibility, toughness and adhesion) [2].

Ormocers®

The Ormocers® materials (ORganic MOdified CERamics) are developed by the Fraunhofer Institute and made commercially available by micro resist technology [15]. They are an example of an inorganic / organic material. The first step of the Ormocers® synthesis is a hydrolysis/condensation reaction of functionalized alkoxysilanes and leads to the formation of organically modified inorganic nanoscale oligomers. Their size and shape can be influenced easily by modifying the polycondensation conditions ([16]). The second processing step after the addition of thermal- and/or photoinitiator contains a polymerization reaction, leading to a fully crosslinked three dimensional network. This is one of the reasons for the good structure accuracy up to temperatures of 270^{o}C in comparison to conventional thermoplastic materials. The Ormocers® materials have been developed to come as ready to use photosensitive mixtures. This flexibility of the process enables one to adjust the polymers to particular application parameters. Refractive indexes can be tuned over a wide range by mixing various resins. Fig 2.2 shows the structural composition of the material.

They have been proven to combine very good optical and dielectrical properties in the lower high frequency region, which makes them promising candidates for electro-optical applications. They have low transmission losses in the near infrared range for the wavelengths 830 nm, 1310 nm and 1550 nm. The material processing is compatible to conventional equipment in thin film processing, and Ormocers® adhere very well on most substrates such as (metalized) Si wafers, inorganic glasses, polymers, and FR4 material.

Table 2.1: Main properties of Ormocers®

Optical properties	
Propagation loss core material @ 633nm	0.06 dB/cm
Refractive index core	1.538
Refractive index cladding	1.5214
Thermal properties	
Coefficient of thermal expansion	100-130 ppm/K
Thermal stability	up to 270^{o}C

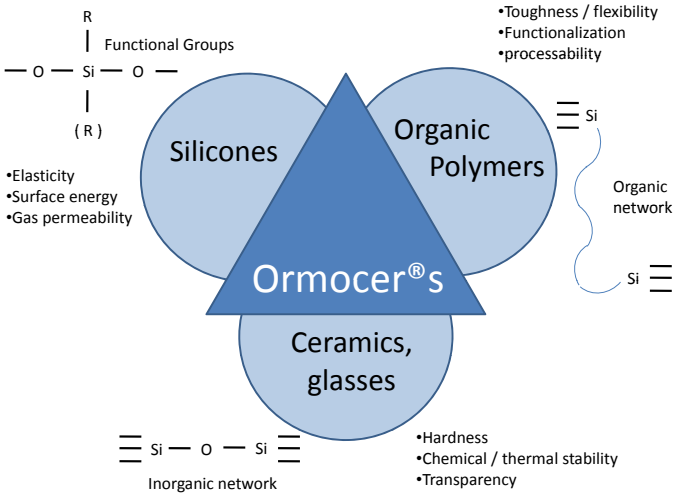


Figure 2.2: Structural composition of the Fraunhofer Institute Ormocers® .

Truemode™ Backplane Polymer

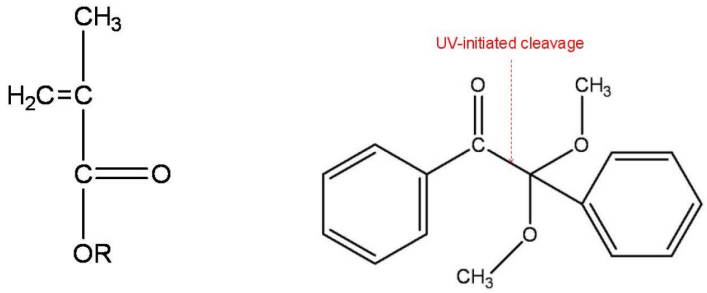
The Truemode™ Backplane Polymer family is a range of multi-functional acrylate polymers for the fabrication of low cost and high performance optical interconnects. The polymers offer a unique combination of low loss, wide-range of refractive index, photo-sensitivity, and environmental stability. They are specifically designed to be compatible with PCB manufacturing including lamination, metal coating and reflow soldering applications.

Table 2.2: Main properties of Truemode™ Backplane Polymer

Optical properties	
Propagation loss core material @ 850nm	$\leq$ 0.04 dB/cm
Refractive index core	1.5266
Refractive index cladding	1.5642
Thermal properties	
Coefficient of thermal expansion	60 ppm/K
Thermal stability	up to 350^{o}C
Glass Transition Temperature(T_g)	180^{o}C

The materials are developed by Exxelis Ltd. (UK) [17]. They have a low optical loss at 850 nm, a high thermal stability (with Tg higher than 150^{o}C and decomposition temperature higher than 350^{o}C) and an excellent adhesion to common

substrates. The high T_g is a consequence of the highly cross-linked nature of the material. From the datasheet we do know the main optical and thermal properties, which are listed in Table 2.2. It is a photo-sensitive material that is polymerized using a radical addition polymerization reaction, which means that an initiator is used to start the polymerization reaction. The initiation is done with a UV-initiator (Irgacure 651). The basic structure of the photo-initiator is shown in Fig 2.3.



(a) (b)

Figure 2.3: Basic structure of methacrylate (a) and of the photo-initiator Irgacure651 for the Truemode™ Backplane Polymer material.

The photo-initiator can be split into two radicals by the UV-induced cleavage. The UV-exposure however has to be done in an inert environment such as nitrogen or vacuum in order to prevent inhibition by oxygen molecules present in standard environment.

The above described material is the original Truemode™ Backplane Polymer material, which we will refer to as the wet film formulation. The core material is also available in a dry film formulation, which can be UV-exposed in contact mode in standard environment, allowing the use of the available mask-aligner at CMST Microsystems.

Epocore / Epoclad

The Epocore/Epoclad material has been developed as a new material for PCB optical waveguides (Microresist [15]). The material can be patterned with standard photolithography and is compatible with the elevated temperature and pressure that occur during standard PCB manufacturing [18]. The material can be UV-exposed in contact mode, meaning that the mask pattern can be imaged onto the optical layer in a very reliable way. The optical loss at 850 nm wavelength is

higher than the other polymers that have been studied, around 0.2 dB/cm, but is acceptable for links with a limited length. Epoxy resins only reach their final properties as reactive resins after they have successfully undergone final curing. As the degree of crosslinking increases, the glass temperature of a polymer rises, and, therefore too, the temperature necessary for curing. This is also true for the modified resist materials EpoCore and EpoClad. Table 2.3 shows the main properties of this Epocore / Epoclad material.

Table 2.3: Main properties of Epocore / Epoclad

Optical properties	
Propagation loss core material @ 850nm	$\leq$ 0.2 dB/cm
Refractive index core	1.58
Refractive index cladding	1.57
Thermal properties	
Coefficient of thermal expansion	14-16 ppm/K
Thermal stability	up to 230^{o}C
Glass Transition Temperature(T_g)	180^{o}C

LightLink™

LightLink™ is a material from the silsesquioxanes family developed by Rohm and Haas [19]. They claim these materials have a significant promise in the optical interconnection market due to their photoimaging, optical, hydrophobic and thermal stability properties. The material is schematically represented in Figure 2.4 and lends itself to numerous configurations where R1, R2, R3 and R4 can be a combination of aliphatic and/or aromatic groups. Depending upon the functional groups attached to the polymer backbone, various performance factors can be designed into the material, including dissolution rate, mechanical properties and optical loss.

The siloxane nature of the LightLink™ waveguide system minimizes the intrinsic optical loss for 850 nm applications. Surface roughness after processing is less than 40 nm, which minimizes extrinsic optical waveguide loss due to the lithographic processing. The main properties of LightLink™ are shown in Table 2.4. The Coefficient of Thermal Expansion (CTE) is not provided by Rohm and Haas or in literature.
The LightLink™ material can be processed on a wide range of substrates, including silicon, copper and epoxy-based substrates as FR4. The material also shows good planarization behavior. The undercladding layer can eliminate the underlying copper layer roughness completely and can lower the macro-roughness of weaved FR4 boards to 50%.

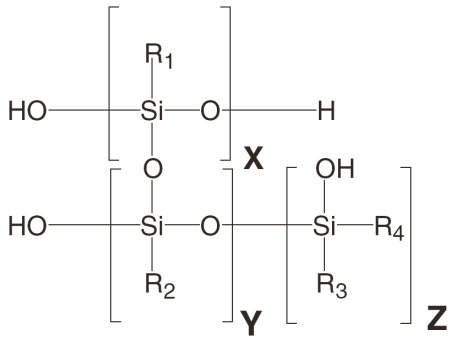


Figure 2.4: Inorganic / organic polymer backbone of LightLink™ .

Table 2.4: Main properties of LightLink™

Optical properties	
Propagation loss core material @ 850nm	0.049 dB/cm
Refractive index core	1.512
Refractive index cladding	1.490
Thermal properties	
Thermal stability	up to 350^{o}C

2.3.6 Group O-F-P: Optical, flexible and Process compatible materials

Most of the available optical waveguide materials were developed with the idea of creating low loss, versatile manufacturable, high reliable waveguides on rigid boards using standard PCB manufacturing tools and processes. Mechanical flexibility was not a restraint, meaning that the materials from Group O-P are not flexible enough.
During the last 4 years, few of the material suppliers started modifying their materials to fulfill the demand for flexible variants. This was often done within the frame of a research project or in close collaboration with a research center. The resulting materials are therefore at this moment still very expensive and often limited available. Following companies have claimed to be successful in realizing flexible waveguide polymer material:

- Chemoptics Inc. [31]
- Rohm & Haas [19]
- Optical Crosslinks [36]

Table 2.5: State-of-the-art flexible waveguides materials, fabrication and characterization Table Part 1

Nr.	Publi-cation date	Research institute / Company	Material family name (core , cladding) name	Core material provider / name	Core refr. index	Clad material provider / name	Clad refr. index	Δ n (%)
1	2009	IBM	Polysilsesquioxanes	XP-6701A	1,51	XP-07423A	1,48	2,0
2	2009	Dow Corning	siloxane based	OE-4140	1,52	OE-4141	1,50	1,3
3	2007	OPERA	ATMS & FBPA sol-gel		1,5		1,45	3,3
4	2008	NTT Photonics	Epoxy					
5	2005	CRC Canada	fluorinated poly(arylene)ether					1,3
6	2009	NCSR Greece	fluorinated methacrylate					0 - 4,2
7	2004	Univ Dortmund	PDMS	SLM 77522	1,43	RT-601	1,41	1,4
8a	2008	Korea Photonics	acrylate	ChemOptics Inc.	1,54446	ChemOptics Inc.	1,5227	1,4
8b	2008	Korea Photonics	acrylate		1,5306		1,5072	1,5
8c	2009	Korea Photonics	(Polyether sulfon, Epoxy)		1,65		1,625	1,5
8d	2008	Korea Photonics	acrylate	ChemOptics Inc.	1,546	ChemOptics Inc.	1,5227	1,5
8e	2007	Korea Photonics	fluorinated methacrylate	Hybrimer	1,51	Hybrimer	1,48	2,0
9	2006	ChemOptics	acrylate	FOWG-106	1,547	FOWG-107	1,523	1,6
10	2005	KAIST Korea	polysiloxane	Hybrimer	1,536	Hybrimer	1,501	2,3
11	2002	Mitsui Chemicals	fluorinated polyimide					0,5
12	2007	Loughborough Univ	Polyimide and LCP					
13	2006	ADEKA	nano-hybrid silicone		1,521		1,499	1,4
14a	2000	AlliedSignal	acrylate					
14b	1996	AlliedSignal	acrylate					
15a	2008	OXL	acrylate	Guidelink		Guidelink		0,2 - 2,3
15b	2008	OXL	acrylate	Guidelink		Guidelink		
16	2008	Unimicron Singapore	fluorinated acrylate	WIR30-RI	1,5	WIR30-RI	1,48	1,3
17	2005	Nitto Denko	Epoxy	Flexwin	1,615	Flexwin	1,593	1,4
18	2008	Matsushita	Epoxy					
19	2009	RPO	inorganic polymer glass (IPG)					
20	2005	Toronto Univ.	(glass, silicone)					
21	2008	JSR Corporation	acrylate		1,539		1,491	3,1
22	2002	VTT	ormosils					
23	2007	NEC Japan	alicyclic monomers		1,532		1,515	1,1
24a	2002	Texas Univ.	photosensitive PI	Amoco Chemicals		Amoco Chemicals		0,7
25b	2004	Texas Univ.	(SU-8, Topas film)					
25c	2004	Texas Univ.	perfluorinated acrylate	ZPU12-460		ZPU12-450		
25d	2005	Texas Univ.	perfluorinated acrylate	WIR30-470	1,47	WIR30-450	1,45	1,4
25e	2008	Texas Univ.	perfluorinated acrylate	WIR30-470	1,47	WIR30-450	1,45	1,4
26	2008	Georgia Tech	(IPG, Siloxane Epoxy)	RPO	1,52	siloxane epoxy	1,49	2,0
27	2002	Nortel	Polyimide					
28	2008	Omron	acrylate+polyurethane mix					0,4
29	2008	ETRI Korea	(Epoxy, PMMA)		1,543		1,49	3,4
30	1995	Honeywell	(Polyetherimide, BCB)		1,65		1,55	6,1

Table 2.6: State-of-the-art flexible waveguides materials, fabrication and characterization Table Part 2

Nr.	optical loss (dB/cm)	wavelength nm	Waveguide fabrication method	WG dimensions (μm x μm)	Minimum bending radius (mm)	Bending loss "@" bending angle "@" bending radius	cross talk (dB)	Reference
1	0,05	850	direct laser writing	40 x 50	4			[20]
2	0,04	850	photolithography / wet developing	50 x 50			-30	[21]
3	0,32	850	UV embossing	50 x 50	1	1dB @ 180^o@ 2 mm		[2]
4	0,06	850	stamping	40 x 40	1	1dB @ 180^o@ 3,5mm		[22]
5	0,8		RIE	6 x 6				[23]
6								[24]
7	0,035	850	casting	70 x 70				[25]
8a	0,24	850	dry etch	50 x 50	3	3,7 dB @ 360^o@ 3mm	-35	[26]
8b			UV imprint	50 x 50	1	1dB @ 180^o@ 4mm		[27]
8c	1,3	850	channel sawing	100 x 100		2 dB @ 360^o@ 3mm		[28]
8d	0,24	850	dry etch	50 x 50	1	1dB @ 180^o@ 5mm		[29]
8e			UV embossing	60 x 60				[30]
9	0,1	850	photolithography / wet developing					[31]
10	0,24	850	UV soft lithography	60 x 90	2	1dB @ 180^o@ 2mm		[14]
11	0,36	850	moulding	15 x 15				[9]
12			printing					[32]
13	0,1	850	photolithography / wet developing	50 x 50	1	$\leq$1dB @ 180^o@ 1 mm		[33]
14a			varia					[34]
14b	0,02	840	laser direct writing					[35]
15a	0,08	840	light induced self developing		1	0,1dB @ 90^o@ 5mm		[36]
15b	0,08	840		50 x 50		$\leq$1dB @ 180^o@ 4mm		[36]
16	0,3	850	soft molding	70 x 70				[37]
17	0,1	830	photolithography / wet developing	50 x 50			-30	[38]
18	0,1	850		40 x 40				[39]
19			dry etch					[40]
20	6		laser direct writing	15 x 15	4	1dB @ 180^o@ 4mm		[41]
21	0,15	850	dry film/litho	50 x 50	1	$\leq$1dB @ 360^o@ 1mm		[42]
22			UV imprinting					[43]
23	0,13	850	photolithography / wet developing	50 x 50			-40	[44]
24a	0,21	850	photolithography / wet developing	50 x 50			-32	[7]
25b	0,6	850	casting	50 x 50				[45]
25c	0,3	850	casting	50 x 50				[46]
25d	0,156	850	casting	50 x 50				[47]
25e	0,09	850	UV embossing	50 x 50				[48]
26	0,24	1320		50 x 62		0,12dB @ 90^o@ 12mm		[49]
27	2	1320	RIE	2 x 2				[8]
28	0,07	850	UV embossing	40 x 40	1	$\leq$1dB @ 180^o@ 1mm		[50]
29	0,1	850	hot embossing	50 x 50		0,1dB @ 90^o@ 10mm		[51]
30	0,24	830	RIE	25 x 25	¡3	$\leq$1dB @ 180^o@ 3mm		[52]

- Nitto Denko [38]
- Omron [50]
- Fuji Xerox Co.,Ltd [53]
- Matsushita [39]
- AlliedSignal Inc. [34]
- RPO Inc.[40]

We believe this list is far from complete.

More detailed information on the flexible materials of these itemized providers is given below:

Exguide^{TM} FOWG series from Chemoptics Inc. [31]

The FOWG series are photoactive UV curable resins based on acrylate. They are applicable to flexible substrates. The patterning of the waveguides is done with photolithography and wet development. These resins have low optical loss at near 830nm wavelength ($\leq$ 0.1 dB/cm at 830 nm) , small birefringence and excellent environmental stability. To obtain the best film quality, a nitrogen environment is recommended during the UV exposure time. Figure 2.5 shows a picture of flexible waveguide, fabricated with the Exguide^{TM} FOWG waveguide resin series.

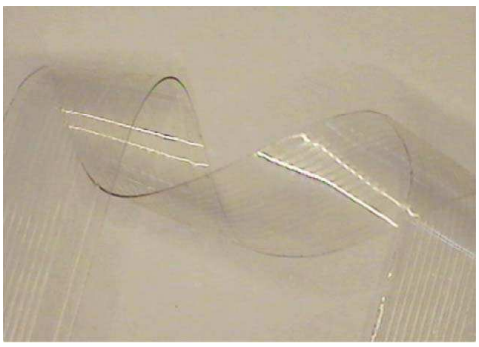


Figure 2.5: Flexible Exguide^{TM} FOWG waveguide resin series from ChemOptics Inc.

The refractive indexes of core and cladding are 1.547 and 1.523, measured at a wavelength of 830 nm.The glass transition temperature is 30 to 50 ^{o}C and the degradation temperature 280 ^{o}C.

LightLink™ XP-07423A series from Rohm & Haas [19]

The LightLink™ XP-07423A series are a modified flexible version of the earlier rigid LightLink™ XP-5202A cladding series. The rigid version is the one discussed in Section 2.3.5, which is used in this PhD work. The optical waveguide losses of this flexible LightLink™ is 0.05 dB / cm at a wavelength of 850 nm. The waveguides can be bent to a bending radius downto 4 mm. The core used for this, is the XP-6701A series. Refractive indexes of core / clad is 1.48 / 1.51.

GuideLink^{TM} from Optical Crosslinks [36]

The GuideLink^{TM} flexible optical waveguides are made from an acrylate based polymer and are commercially available as finished waveguide stack, with or without connector attached. They are fabricated by laminating pre-coated cladding layers with the core layer. The waveguide patterning is done using a light induced self development step, based on the internal diffusion of monomers at low temperatures (15 to 45 ^{o}C), followed by photo and thermal fixing. This results in very smooth sidewalls of the waveguide since the side walls are defined by monomer diffusion and the waveguide top and bottom are defined by the coated film surfaces that are flat to tens of nanometers. The loss in the waveguides (0.08 dB / cm) is almost as low as the bulk losses. A 90 degree bend with bending radius 5 mm results in a loss of 0.1 dB. The core / cladding refractive indexes are 1.485 / 1.51. The waveguides have Tg of 145^{o}C and sustain a 260^{o}Csolder spike and a 2 week storage at 125 ^{o}C.

FlexWin series from Nitto Denko [38]

Nitto Denko developed a photo-sensitive Epoxy with excellent transparency, flexibility and manufacturability. Waveguide patterning can be done using a single UV-lithography step, wet developing and thermal curing. The resulting Epoxy waveguides show an optical propagation loss lower than 0.1 dB / cm at 850 nm. The core / cladding have an RI of 1.593 / 1.615 and the waveguides are thermally stable upto 260^{o}C. The waveguide foil can be bended to a bending radius of 1 mm without damaging.

Omron [50]

Omron presented a flexible optical datalink in the hinge of a cell phone. The material of the waveguides consists of a self-developed mix of acrylates and polyurethane. Optical propagation losses of multimode waveguides are 0.07 dB/cm and bending loss below 0.2 dB for a 360 degrees 1 mm bending radius bend. The waveguide stack is very strong and tear resistant. The patterning of

the waveguide was done using a stamping technique. The degradation temperature is above 200 ^{o}Cand the relative index difference 0.42 %.

Matsushita [39]

Matsushita Electric Works Ltd developed an optical-waveguide film material for printed-circuit boards (PCB) equipped with both electric and optical circuits and a processing method for the material. It is possible to transfer signals at 10 Gbps with a 1m circuit. Before this film material was developed, only about 10cm of optical waveguide had been confirmed to be practical. The prototyped PCB is as large as a Japanese post card (148 x 100mm) and spirally printed with a 1m-long optical waveguide whose cross section measures 40 x 40m. When 850 nm wavelength light is used, the loss of the optical circuit including the mirrors at the both ends of the optical waveguide is 12 dB. The film material is made of epoxy resin and can be used for both rigid and flexible substrates. Its linear loss is less than 0.1 dB/cm, and the loss in the mirror parts is 0.5 dB. The company plans to provide PCB manufacturers with the film material and the method to process optical waveguides. It aims to achieve the practical use of the film in 2010 or 2011.

AlliedSignal Inc. [34]

The flexible waveguide material developed by AlliedSignal Inc.is based on combinations of multifunctional acrylate monomers and oligomers together with various additives. These polymers are particularly suitable for practical low-loss optical devices because acrylates intrinsically have relatively low stress-optic coefficients and because photochemical processing directly from monomers provides polymers characterized by relatively low internal stress. This combination of materials properties allows the creation of waveguides that exhibit both low scattering losses and low polarization dependent losses. Upon exposure to UV radiation, these monomer systems form highly crosslinked networks, which exhibit low intrinsic absorption in the wavelength range extending from 400 to 1600 nm. By blending and copolymerizing selected miscible monomers, the synthetic scheme allows for precise tailoring of the refractive index over a very broad range from 1.3 to 1.6. At the same time, the synthetic scheme allows other physical properties of the materials such as flexibility and toughness as well as such important properties as surface energy and adhesion to be tailored to meet the needs of specific applications.
The bulk absorption loss is 0.001 at 840 nm, the degradation temperature 250 ^{o}C. and the minimum bending radius 0.6 mm. The losses of a multimode are measured to be 0.024 dB/cm.

Inorganic Polymer Glass^{TM} from RPO Inc.[40]

RPOs optical waveguides are made from a proprietary material system, Inorganic Polymer Glass^{TM}. They can control both the optical and physical properties, making them suitable for many applications. The waveguides do not require packaging to protect them from environmental conditions. RPO has developed a low cost waveguide manufacturing technology using photo-resist tools from the LCD industry. This unique approach allows the production of large waveguide sets. In communications, applications include high speed optical interconnects (chip to chip, chip to board, board to board) and LAN and FTTH passive optical components. In sensors, the waveguides can be applied to touch-screens, biochips and other high-value sensor applications.

2.4 Modification of non-flexible materials

Since the lack of existing commercially available flexible optical materials, a cooperation with the Polymer Chemistry and Biomaterials (PBM) Group of the Ghent University [54] was set up within the framework of the SBO project FAOS [1](IWT [55]).

Because Truemode™ Backplane Polymer showed the best usability for the scope of this PhD, the main focus was on the development of polymers or copolymers that can be combined with Truemode™ Backplane Polymer in order to enhance the flexibility of the material after processing. Since the processed material is a polymer network, the aim was to alter the material properties by adding polymers which can improve the final material behavior. A successful optimization of the material properties would lead to better performing materials.
A variety of polymers exists as candidate material to fine tune the Truemode™ Backplane Polymer properties. The materials should certainly possess a low (below room temperature) Tg (glass transition temperature). This leads to materials which are flexible at room temperature. Mixing of these polymers or copolymers with Truemode™ Backplane Polymer should lead to materials with an enhanced flexibility. Another requirement is that the materials should withstand the processing temperatures of Truemode™ Backplane Polymer which are typically above 200^{o}C.
Following systems are under investigation:

- Adding and mixing of linear polymers with a low Tg, which do not actual crosslink with the network, but act as an external weakener in the system. All combinations of PMMAxBuMA (PolyMethylMethAcrylate - ButylMethAcrylate)and PMMAxEHMA (PolyMethylMethAcrylate - EthylMethylAcrylate) can be used for this, together with the homopolymers

PMMa (PolyMethylMethAcrylate), PBuMA (PolyButylMethAcrylate) and PEHMA (PolyEthylMethylAcrylate). The low Tg and stability of these systems were confirmed with differential scanning calorimetry and thermogravimetric analysis respectively.

- Adding and mixing of crosslinkable chemical networks. This is again a methacrylate based system where the synthesized polymers contain a sidechain with functionalities. These polymers can than be crosslinked with the system, resulting in a higher stability and better mechanical properties.

- Adding and mixing of PEGdimethacrylates together with monomers. PEGdiMA is a crosslinker, so the system can be crosslinked very fast and the methacrylates are again crosslinked with the system.

The thus developed materials and mixtures are characterized mechanically. A 1mm thick material sample is fixed between two plates with a hole. At the location of the hole, a perpendicular force is applied to the material. The elastic modulus can be derived from the relationship between the applied force and the material deformation and is shown in Fig. 2.6 for PMMAxBuMAy and PMMAxEHMAy for different mol% MMA.

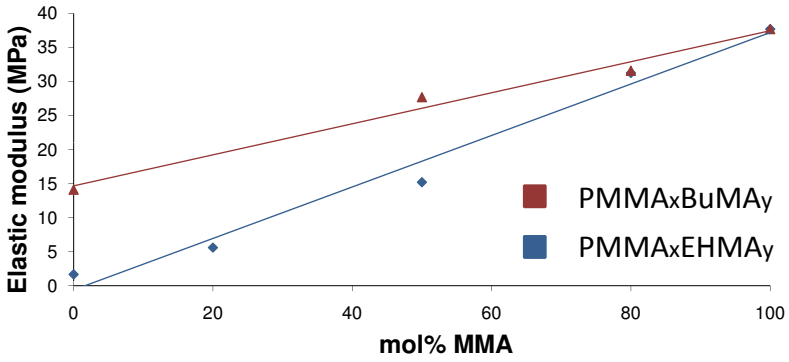


Figure 2.6: Elastic modulus of PMMAxBuMAy and PMMAxEHMAy.

The compressive modulus is measured using a cylindrical sample (diameter 5 mm and height 6 mm). The relationship between pressure and compression shows us the compressive modulus. The tensile modulus of the materials is measured using a 1 mm thick dogbone shaped material sample which is clamped at both ends. The relationship between the stress on the sample and the strain defines the tensile modulus. The compressive and tensile modulus for the investigated materials and mixtures is shown in Fig 2.7.

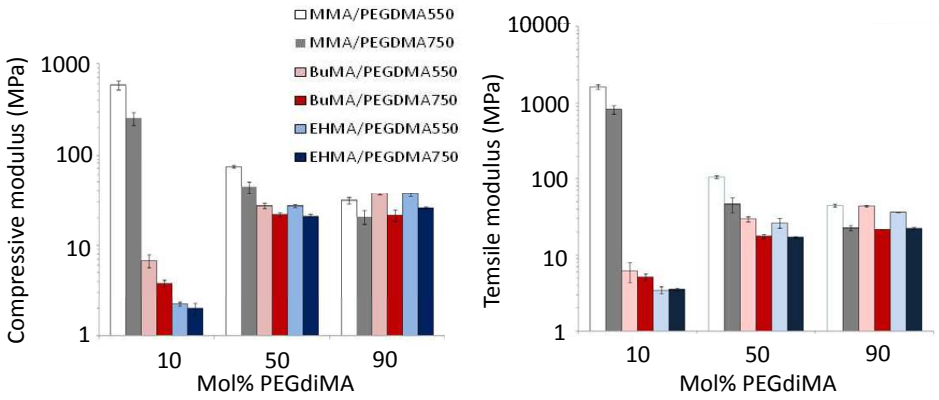


Figure 2.7: Compressive modulus and tensile modulus of the investigated mixtures/materials for different mol% PEGdiMA.

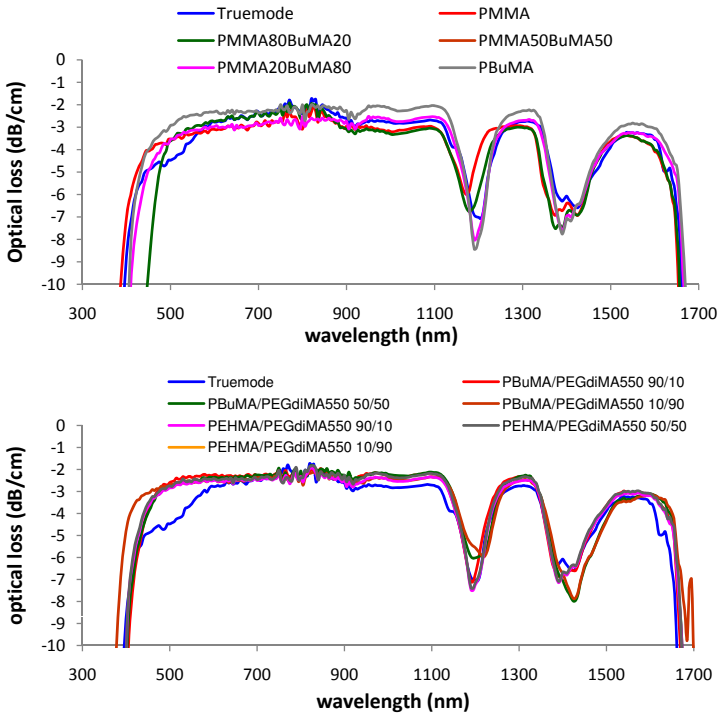


Figure 2.8: Optical bulk losses of Truemode™ Backplane Polymer material and the different mixtures/materials.

In case of the MMA mixture: an increasing amount of PEGdiMA results in a decreasing modulus, which can be explained by the fact that the PEG chain is less rigid than the PMMA chain. The PPMA contains only short sidechains, which limits the moveability in the system, and thus the flexibility of the material. In case of the BuMA and EHMA, we can see the opposite. The BuMA and EHMA are already quite flexible. The adding of PEGdiMA only enhances the amount of crosslinks in the system, and thus decreases the flexibility because of the higher density of the system.

Optical bulk loss measurements were performed on the different materials and mixtures and compared to the losses of plain Truemode™ Backplane Polymer material. Fig. 2.8 shows the results. We can conclude from the measurements that the mixing of the different components has no major influence on the optical absorption of the material.

Fig. 2.9 shows the visual comparison of the flexibility of the different developed mixtures/materials by bending a 1 mm thick material sample.

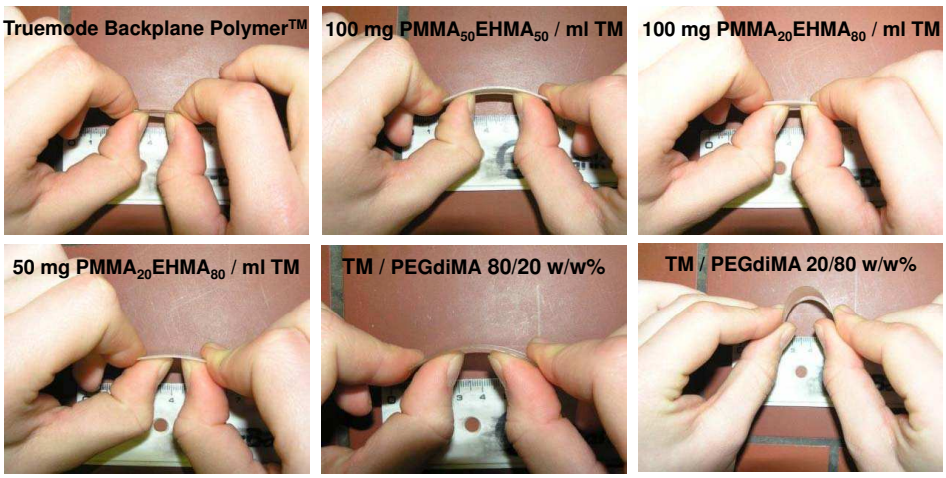


Figure 2.9: Visual comparison of the flexibility of the differnt developed mixtures materials.

The follow up of the cooperation with the PBM Group is established within two running PhD thesis's at CMST Microsystems (Jeroen Missinne [56] & Bram Van Hoe [57]).

2.5 Conclusions

The flexible optical waveguides presented in this PhD work and the embedded active optical links should be fabricated in a well chosen material. There are no leading materials in this relatively new, fast growing market at this moment but a large variety of materials from total different material families is available. Organic-inorganic materials are newly developed within this research area to combine the thermal, mechanical and optical properties of organic and inorganic materials with good results in literature. The requirements upon the material to be used in this PhD research were unraveled in different parameters. A few commercially available optical materials meet these requirements except the need for flexibility. More flexible materials lack in availability. Therefore we choose to work with commercially available non-flexible materials (Truemode™ Backplane Polymer , LightLink™ , Epocore / Epoclad and Ormocers®) which were described superficially in this chapter. The flexibility of these non-flexible materials can be significantly enhanced by using mechanical support layers as will be investigated in Chapter 4. As an ongoing alternative, chemical modifications are being made to these materials to improve their flexibility.

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Chapter 3

Parallel optical waveguides

This chapter focuses on the board level, where the state of the art of optical communications has revealed the many advantages of polymer optical multimode waveguides. The different waveguide fabrication possibilities with different waveguide materials (see Chapter 2) are discussed, followed by an intense study of photolithographic waveguides, with special focus on layer deposition, curing, layer uniformity, reproducibility, waveguide profile, side wall roughness's and planarization. This research has the main intension to have good control over the waveguide fabrication process since later in this work, active components and coupling elements will be integrated herein with high positioning requirements.

3.1 Introduction

The use of waveguides brings an attractive alternative to using optical fibers as a replacement for traditional flexible copper interconnects. When compared to fibers, waveguides are a more versatile solution and have the potential to be lower in cost. In the 1940s Paul Eisler was credited with the revolutionary inventing of printed circuit boards to replace wires in electronic circuitry [1]. Before the use of printed circuit boards, electrical interconnects consisted of copper wires which were very bulky and difficult to manage especially when the designs became complex. The invention of printed circuit boards revolutionized electronics and computing through manufacturing, performance and cost gains. In a similar way, the use of waveguides can do the same for optical communications. For optical data links, people have considered various approaches, essentially all based on pieces of fiber, going from discrete optical fibers, to optical fibers laminated into flexible foils or into boards. An illustration of a discrete fiber based optical layer is given in Figure 3.1, showing an application board on which optical sig-

nals, coming from the optical backplane are routed to micromechanical all-optical switches and back to the backplane connectors [2]. The limitation of optical fibers minimum bending radii, the cost of terminating and connecting of separate fibers and the fragility of such boards, makes them very unattractive. Introducing polymer waveguides offers the possibility to route all the optical signals in one thin plane, extendable to multi-level routing [3]. Optical waveguides also enable extra functionalities like splitting, multiplexing, crossing, tapering, low bending radii curves, etc.. The whole optical routing system can be fabricated in one single polymer waveguide core patterning step, reducing fabrication costs drastically.

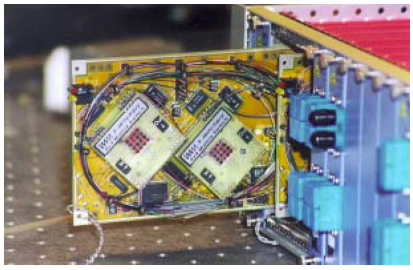

Figure 3.1: Fiber based optical interconnections integrated in a PCB (source: ACTS PLATO Project)

The transition from rigid optical waveguides to flexible waveguides is a very new trend of the past 4 years. Introduction, rationale and applications of these flexible waveguides is extensively described in the introduction chapter (Chapter 1) of this thesis.

In [4, 3], the realization and characterization of optical waveguides in Truemode™ Backplane Polymer and Ormocers® material was discussed using laser ablation as fabrication technique. This chapter is an addition to these two PhD thesiss's by looking into the photolithographic waveguides rather than their laser ablated counterparts. The focus will also be more on the reproducibility and the planarization of the layers within the waveguide stack. Also new materials as LightLink™ and Epocore / Epoclad are introduced.

3.2 Waveguide fabrication techniques

The fabrication of optical waveguides can be done with a wide range of techniques which are all characterized in the past. The state-of-the-art on this field from three years ago is discussed in detail in the PhD thesis of Geert van Steenberge [4]. Table 3.1 shows an overview of these techniques with their main advantages and disadvantages.

For the fabrication of flexible optical waveguides, every process used for rigid waveguides can be used as well. During the core patterning process steps, which actually form the waveguides, the flexible substrates are often transformed temporary into rigid substrates. Different approaches are possible. When fabrication OPCB's (Optical Printed Circuit Boards) sheet to sheet, the flexible substrate can be attached to reusable temporary carriers like glass, FR4 and silicon wafers by using release layers or peel-off adhesives. When using roll-to-roll fabrication processes, the flexible foils are supported by cylinders or hard supporting tables to do the patterning locally in a rigid way.

Table 3.1: Overview of existing waveguide fabrication methods for rigid optical polymer waveguides

Fabrication method	Advantages	Disadvantages
Photolithography + wet developing	High resolution	High cost for large area masks
Laser direct writing	Flexible technology	Low throughput
Diffusion + photolocking	No chemicals needed High planarity	Limited suitable materials
Moulding / Stamping / casting	Low cost	Higher sidewall roughness
Laserablation	Flexible technology	Low throughput
RIE dry etching	Applicable on many materials	High cost and sidewall roughness
Channel sawing	Cheap	Poor quality No waveguide bends
Printing	Flexible, cheap	Under development

Some fabrication approaches however have additional advantages in comparison to others when working on flexible substrates. Roll to roll processes benefit

from a continuous production speed, which pushes laser direct writing and diffusion with photolocking to be the most desired production processes. Since cost and large area processing is even more significant in the world of flexible electronics, moulding process is widely applied here. Table 2.5 in Section 2.3.5 in Chapter 2 shows the list of publications on realized flexible optical waveguides and shows that moulding (in the appearance of casting, stamping, soft moulding, UV molding, imprinting, UV embossing or hot embossing) is indeed the most common approach. For the production of straight waveguides on foil, the highest throughput and dimensional stability is obtained with the monomer diffusion and photolocking process. Optical Crosslinks™ [5] uses this technique for mass production of waveguide foils named "Guidelink" with Duponts trademark "Polyguide" process.

The research in this PhD work focusses on the embedding of opto-electronics and waveguides in a flexible foil. The waveguides are playing a key role in this work, but the fabrication process itself is of less importance. In what follows we chose to use photolithographic formed waveguides as proof of principle. The process is described in detail and the reulting waveguides are characterized in thi Chapter. We would like however to point out that any other waveguide fabrication technique can be used in the proposed technology.

3.3 Photolithographic optical waveguide production

This section describes the different process steps for the realization of these waveguides. The process consists mainly of creating a stack of a cladding-layer (undercladding), a core-layer and another cladding-layer (uppercladding). Isolating tracks in the core-layer and consequently surrounding the track completely with cladding material, results in the creation of optical waveguides. This is a well proven principle for optical interconnections on rigid boards. Light that will be coupled into these waveguides will be guided in that layer due to total internal reflection, caused by the different refractive indexes of the core- and the cladding layers.
For this section, we will only focus on rigid substrates since the application of flexible substrates is explained in Section 4.6 in Chapter 4.

3.3.1 Substrate preparation

The rigid substrate is chosen to be standard FR4, since the commercially available optical material are all developed to have good adhesion to this kind of epoxy-based substrates. The FR4 boards are 4 by 4 square inches when they are purchased and are cut into 4 pieces of 2 by 2 square inch size. This size was chosen

for this research because of the compatibility with present infrastructure and the high cost for large dimension substrates. They are than cleaned mechanically by a nitrogen flow outside the clean room and cleaned chemically inside the clean-room by a consecutive acetone, IPA / acetone and IPA rinse. To ensure the out-gassing of these cleaning compounds out of the FR4, the samples are put in the oven on 150 degrees for half an hour. Table 3.2 gives an overview of these process steps.

Table 3.2: FR4 substrate preparation

FR4 substrate preparation	
Process step	Process details
Substrate dimensioning	Sawing
Mechanical cleaning	Nitrogen flow
Chemical cleaning	Acetone bath, 5 minutes, stirring
	50% Aceton / 50% IPA bath, 5 minutes, stirring
	IPA rinse
Drying	150 ^{o}C, 30 minutes

3.3.2 Undercladding layer

Spin coating

Applying of a uniform layer of fluid material over the whole substrate can be performed in many ways (Spin Coat, Ink jet print, Roller coat, Doctor blade, Curtain coat, Screen print, Dip coat, Dry film). With the material characteristics, the low volume fabrication and the possibilities at CMST in consideration, the choice for spin coating was made.
The material that needs to be spin coated is deposited in the middle of the substrate. By spinning this substrate around its middle point, the material will be spread over the complete surface. The deposition of this material should be done with care since any enclosure of dust particles or air bubbles will result in a layer defect. One can make a separation of deposition process following the viscosity of the material:

- Low viscosity 0-5 Poise(eg. Truemode™ Backplane Polymer , LightLink™): Because of the high surface tension of low viscosity materials, the formation of drops is inevitable during spinning. This means that the material will not spread equally over the surface, but will form drops which are ejected of the substrate when they reach the substrate edge, leaving some areas uncovered. To avoid this to happen, one should spread the material over the complete substrate by tilting it in all directions before the spin coating process. The spinning will then thin down the layer to its final thickness.

- Medium viscosity 5-40 Poise (eg. Ormocers® , AZ4562 photoresist): No special precautions must be taken.
- High viscosity $\geq$ 40 Poise (eg. Polyimide, SU-8, Epocore / Epoclad): These materials are very sensitive to air inclusions. Any stirring or handling of the material with syringes or pipettes can result in air inclusions which results in layer defects. Controlled vacuum dispensing systems resolve this problem in automatic dispenser tools. However manual dispensing can only be done airbubble-free by pouring directly from the bottle to the substrate. To prevent the contamination of large amount of material, one should divide a large bottle of material in more little ones. Stirring, mixing or pouring in another recipient should be avoided. If one of these actions must be done, the air bubble insertions can be removed afterwards by putting the material at elevated temperature (well below curing temperatures) for a whole night.

The spinning process is the same for all materials: the substrate with an adequate amount of the spin-coating material is put on a vacuum chuck which holds the sample into place during spinning.

A clean back side of the sample is necessary to assure a sufficient vacuum. Therefore the backside of the sample must be cleaned after each layer deposition. Especially high viscosity materials tend to leave trails of material at the backside during spinning.

Edge bead

When spincoating fluid materials, edge bead is a common phenomenon. Due to the extra surface energy at the edge of a substrate and the roughness at these sides, more material sticks to the substrate and the layer thickness will be higher than in the middle of the substrate. Figure 3.3 shows a picture of a cross-section which clearly shows this phenomenon. The lower the viscosity of the material, the higher the impact of surface energy differences and thus the higher the edge bead. Figure 3.2 shows the layer thickness at the edge of 8 different Truemode™ Backplane Polymer layer samples, 4 of which no precaution is taken and 4 of which the edge material is removed. The zero value of the Y-axis is the top of the spin-coated layer.

The removal of material at the edges can be done manually with either a tissue for low viscosity materials which absorbs the material or either with a blade to scrape of the excess material. The width of the removed edge material band varies between 4 and 7 mm because of the manual character of the removal, but this has no influence on further processing at all.

In the design of projection masks, one must always keep in mind that the outer 10 mm edge of a sample is never useful for this reason. Functional features should

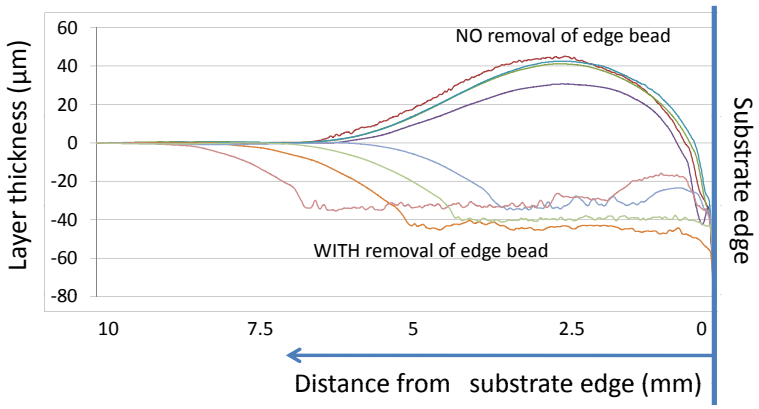

Figure 3.2: Edge layer thickness of wet film Truemode™ Backplane Polymer with and without edge bead removal (target layer thickness = 40 μm)

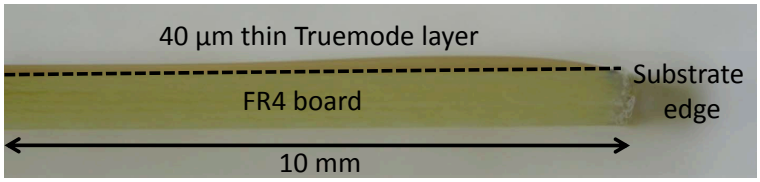

Figure 3.3: Cross-section of a 40 μm Truemode™ Backplane Polymer layer on top of an FR4 substrate with clearly visible edge bead

always be within this 10 mm safety contour. Figure 3.2 shows that the excess layer thickness can go up to 40 μm . For each stacked layer, this thickness will count up and end up at an intolerable value. The main reasons why this edge bead is unfavorable are:

- Photolithographic contact masks used later in the process will not have contact with the material layer that needs to be patterned. This causes unwanted pattern dimension variations.
- The thickness of the material at the corners (where a double edge bead appears) can be so large that the material has difficulties to fully crosslink, resulting in sticky corner material.
- From the moment the spinning of the substrates is actually over, the excess material at the edges will steadily flow back to the center of the sample, which increases the final layer thickness. During the UV exposure, this flow will stop due to cross-linking of the material, but we have no control over this curing speed, so only possibility is the removal of the excess material

directly after the spinning. Once the edge material is removed, the material in the middle does not tend to flow to the edges where there is no material, so once the edge material is removed, the layer thickness is stable over the complete substrate.

Spin speed / Layer thickness

The spin speed has a direct exponential relationship to the material final layer thickness. The physical explanation behind this process is that the material will be pushed away from the middle of the substrate (spinning axis) until the centrifugal force on the material is equal to the cohesion force of the fluid material. This means that the spin speed - layer thickness relationship is different for each material. Higher viscosity materials show higher cohesion forces and thus need higher spin speeds to result in the same layer thickness as low viscosity materials. Figure 3.4 shows the spin speed curves for LightLink™ , Ormocers® , Truemode™ Backplane Polymer and LightLink™ cladding layers on an FR4 substrate. The viscosity of the different materials is discussed in Section 3.3.2.

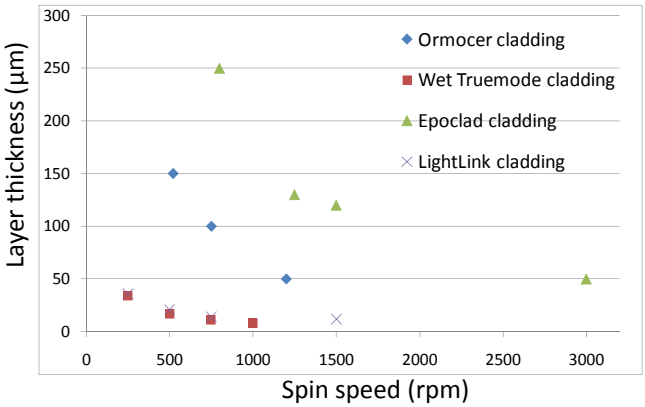

Figure 3.4: Layer thickness versus spin speed for 4 cladding materials on top of an FR4 substrate.

The substrate underneath the layer can influence the final thickness because the substrate surface roughness interacts with the material and adds some extra force elements in the equation above. This influence is however limited. In Figure 3.5, the spin speed curves of a LightLink™ cladding layer on an FR4 board is compared to that of an LightLink™ clad layer onto another LightLink™ cladding layer. The FR4 board has a much higher roughness than a cured LightLink™ cladding layer and results in clearly thinner spincoated layer thicknesses.

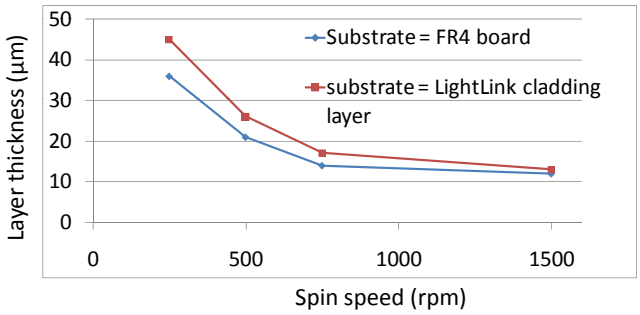

Figure 3.5: Influence of the underlying substrate on the spin speed curve of LightLink™ cladding material.

Planarization

Spincoating a fluidic material on a completely flat substrate results in a very uniform layer. However the substrate to be spin-coated is offen not flat and can have copper tracks, waveguides, trenches, etc. Spin coating on these non-uniformities will result in non-uniform thicknesses of the spincoated layer. This issue is called planarization. Figure 3.6 shows schematically what happens in case of a copper track and a trench.

The film leveling while spincoating is an equilibrium problem. The final film profile is determined when the netto force among capillary, centrifugal, and viscous contributions is zero. The most important parameter during spincoating is the ratio between centrifugal and capillary force. The degree of planarization is also affected by the ratio of the film thickness to pattern height. Also the material shrinkage has an influence: the larger the shrinkage, the larger the degradation of the final film profile.

Table 3.3: Planarization of the undercladding layer for the four investigated optical materials on top of a 17 μm thick, 1.5 mm wide copper track.

Optical material	Spin speed (rpm)	Thickness on FR4 board (μm)	Thickness on copper track (μm)	Layer thickness overshoot (μm)
Ormocers®	1200	50	28	-5
Epocore / Epoclad	3000	50	35	2
Truemode™	250	33	23	7
LightLink™	200	39	23	1

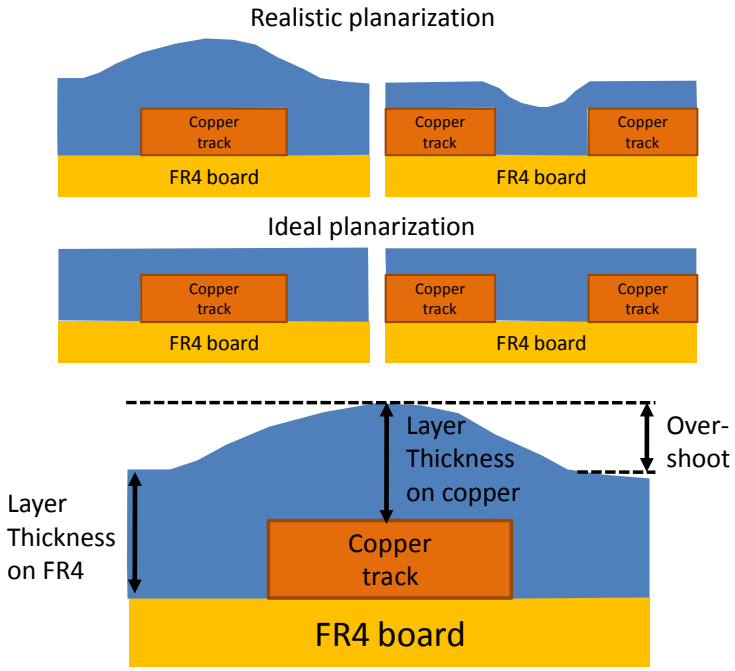

Figure 3.6: Planarization of a polymer spin-coated layer on top of a copper track or trench.

Planarization of spin-coated undercladding layers is of great importance since the waveguides will be fabricated directly on top of this layer, meaning that every irregularity of the undercladding will result in a z-axis bending of the waveguide. Bending of the waveguide results in extra optical losses due to the change in conditions to the law of total internal reflection. Later on in this work, opto-electronic active components and optical coupling elements will be integrated in the undercladding layer. Alignment comes into place here and good control over the z-dimensions becomes really important. Planarization is measured for the four investigated optical materials on top of a 17 μm thick copper track which is 1.5 mm wide. Later on in this work, such copper islands are used as a heat sink for embedded VCSEL's. Table 3.3 compares the cladding layer thickness on the FR4 board and on top of the copper track and shows the layer thickness overshoot for the four investigated optical materials. These parameters are shown schematically in Figure 3.6. It can be seen that the overshoot for the materials is below 10μm . For the Ormocers® material, a negative overshoot is witnessed, which is the result of bad adhesion of Ormocers® to the copper. The Ormocers® tends to contract on top of the copper tracks. When the copper track is a few millimeters wide, the contraction of the Ormocers® is even complete, which means

there will be no Ormocers® material on top of the copper after curing.

Planarization is not only favorable when covering tracks and trenches, but also to eliminate or decrease the periodic surface waves of FR-4 boards. For the application on top of flexible substrates, this is no issue, but since a part of the research is performed on rigid FR-4 substrates, the planarization on this kind of substrates is also investigated and described in what follows:
FR-4 laminates are constructed on multiple plies of epoxy-resin impregnated woven glass cloth. This woven glass structure is experienced as a waved top surface of the FR4 board. Figure 3.7 shows what happens to this waved surface when the FR board is covered with multiple LightLink™ cladding layers. The LightLink™ layers were spin coated with different spin speeds to target a final layer thickness of 40, 50 and 60 μm . The thicker the final layer, the lower the standard deviation of the layer profile. To eliminate the waved surface, one will have to apply quite a thick layer, which is not preferable with respect to cost and processing time. The planarization using the other three investigated materials (Ormocers® , Truemode™ Backplane Polymer and Epocore / Epoclad) shows similar results. We will have to accept the wavy profile, which maximum amplitude is only about 3 μm with a period of 5 mm for a 60 μm thick cladding layer. This results in a maximum surface angle of 0.1 degrees, which is negligible with respect to optical loss in the waveguide on top of the cladding layer.

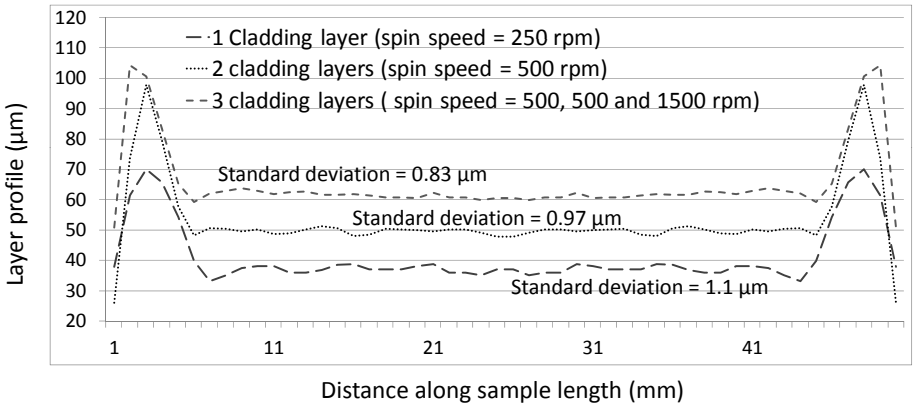

Figure 3.7: Planarization of a waved FR4 surface by spincoating LightLink™ cladding layers.

Layer thickness variation

As depicted in previous subsection, z-dimensions become very important when embedding opto-electronic active and coupling elements in the undercladding layer. That is why planarization needs to be controlled. Not only the planarization defines variations in z-direction, but also the variation in spincoated layer thicknesses. This variation has not been investigated for all the four materials, but only for Truemode™ Backplane Polymer since the embedding of actives and coupling elements later on in this work was only done inside this material. For the fabrication of pure plane waveguides (without any embedded elements), the variation in undercladding layer thickness is of no importance. The thickness deviation results are summarized in Table 3.4. It is seen that layer thickness deviation counts up when stacking multiple layers as expected. Maximum deviations tend to stay within a $\pm$ 12 μm range.

Table 3.4: Truemode™ Backplane Polymer Undercladding layer thickness deviation

Truemode™ Backplane Polymer layer on top of a 17 μm thick copper island (spin speed = 250 rpm)	
Sample population	10 pcs
Average layer thickness	23,0 μm
Thickness standard deviation	2.3 μm
Maximum thickness deviation	4.9 μm
Truemode™ Backplane Polymer double layer on top of a 17 μm thick copper island (spin speed = 250 rpm)	
Sample population	12 pcs
Average layer thickness	54,0 μm
Thickness standard deviation	3.0 μm
Maximum thickness deviation	7.33 μm
Truemode™ Backplane Polymer double layer on top of an FR4 board (spin speed = 250 rpm)	
Sample population	9 pcs
Average layer thickness	61.6 μm
Thickness standard deviation	5.1 μm
Maximum thickness deviation	11.5 μm

Layer material curing

Every spincoated undercladding layer is UV exposed and hardbaked to fully cure the material. UV exposure- and hardbake- duration are chosen following the process sheet from the material providers and optimized in case the curing was not sufficient. These parameters can be found in the optimized undercladding pro-

cess flows of the different materials in Table 3.10.
UV curing of materials is a common approach to get hard cured material because of its great advantages. UV curing can be done solvent free, at room temperature and is known as the fastest way for curing with curing times of a few seconds to 1 minute. Multifunctional acrylate monomers like in Truemode™ Backplane Polymer are UV cross-linked by a photoinitiated radical polymerization. When this process is done in the presence of air, oxygen inhibition becomes a problem. The free radicals formed by the splitting of the photo-initiator are rapidly reacting with O_2 molecules to form peroxides [6]. These groups are not reactive towards the acrylate molecules and can therefore not initiate or participate in any polymerization reaction. For Ormocers® layers, this results in an uncured layer of about 1 μm thickness which can be removed with a dedicated solvent. For Truemode™ Backplane Polymer however, this problems is much more striking, since the layer will not cure at all. An additional amount of photoinitiator or UV energy is therefore needed to consume the oxygen dissolved in the resin, as well as the atmospheric O2 diffusing into the sample during the UV exposure, in order to obtain tack-free layers with the required mechanical properties. Many solutions for this problem were put forward in literature but only one can actually be realized within the CMST lab infrastructure:
Performing the radical photopolymerization under inert conditions prevents any oxygen inhibition. Nitrogen can be used for this purpose. A set-up was available at CMST consisting of a glass box , provided with a hole to fit a nitrogen pistol head. UV exposure is done from above with a constant nitrogen flow through the hole.

Table 3.5: Optimized process flows for the undercladding layer for Epocore / Epoclad , Ormocers® , Truemode™ Backplane Polymer and LightLink™ .

Epocore / Epoclad undercladding layer process flow	
Process step	Process parameters
Spin coat	3000 rpm
Prebake hotplate	60 min. ; 85 ^{o}C
UV exposure	120 s ; 10 mW/cm^2
Post exposure bake hotplate	15 min. ; 85 ^{o}C
Hard bake	60 min. ; 150 ^{o}C
Ormocers® undercladding layer process flow	
Spin coat	1200 rpm
Prebake hotplate	5 min. ; 85 ^{o}C
UV exposure	120 s ; 10 mW/cm^2
Post exposure bake hotplate	5 min. ; 85 ^{o}C
Hard bake	60 min. ; 150 ^{o}C
Wet developing for removal uncured layer	20 s ; MrDev600
Rinse	IPA
Dry	N_2
Truemode™ Backplane Polymer undercladding layer process flow	
Spin coat	250 rpm
UV exposure	60 s in N_2 environment ; 10 mW/cm^2
Spin coat	250 rpm
UV exposure	60 s in N_2 environment ; 10 mW/cm^2
Hard bake	60 min. ; 150 ^{o}C
LightLink™ undercladding layer process flow	
Spin coat	200 rpm
Prebake hotplate	20 min. ; 90 ^{o}C
UV exposure	120 s ; 10 mW/cm^2
Post exposure bake hotplate	10 min. ; 90 ^{o}C
Hard bake	60 min. ; 150 ^{o}C

3.3.3 Core waveguides

Lithographic patterning of waveguides

The deposition of the core material layer happens in a similar spincoating step as the undercladding layer. After the spincoating step and the removal of the edge bead, the layer is baked on a hotplate to remove the solvents (prebake). This results in a dry layer which enables contact lithography. A mask consisting of a 2 mm thick glass plate with a 50 nm thick patterned TiW layer is placed on top

of the dryed core layer, followed by UV exposure. The UV exposure is done on a mask aligner SET MG1410 (see Figure 3.8).

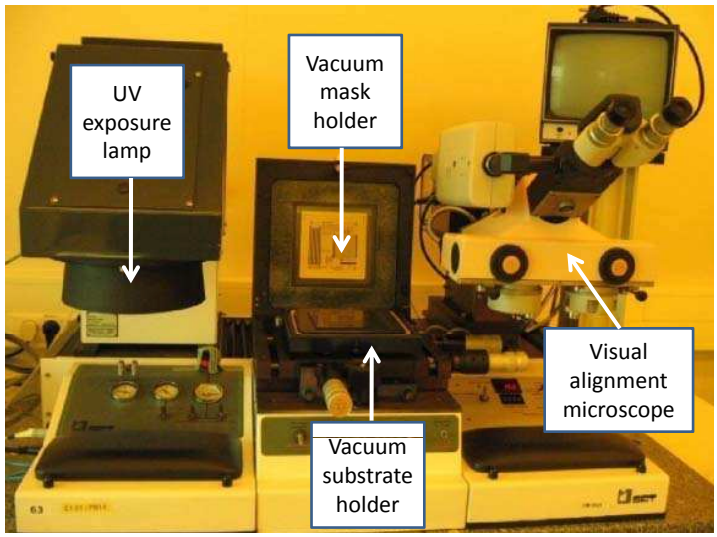

Figure 3.8: Mask aligner SET MG1410 @ CMST Microsystems.

All investigated optical materials act as a negative photoresist. Photo-initiators are mixed inside the optical materials by the providers or by ourselves. At the areas which are exposed to the UV light, the photo-initiator will split into radicals which will attach to the optical material molecules, resulting in preliminary bonding of the molecules and thus cross-linking. This bonding is enhanced by baking the layer on a hotplate at an elevated temperature (post exposure bake). This temperature is high enough to force maximized bonding of the photoinitiators radicals with the optical polymer molecules, but not high enough to realize the mutual crosslinking between the molecules themselves. In a next step the sample is placed in a bath of dedicated wet developer solvent, which will dissolve the spincoated layer except the material which is UV exposed and thus partly crosslinked. Proper rinsing is essential to obtain clear well defined features. This rinsing process is optimized for every investigated material and the rinsing parameters can be found in the optimized process flows in Table 3.8 of the different materials. As a last step, the sample is hardbaked in a convection oven to realize the final crosslinking (curing). A schematic process flow for the fabrication of such a photolithographic optical waveguide is shown in Figure 3.9.

An exception to this process is the Ormocers® material. After prebake, the material is still sticky, which doesn't allow contact UV exposure. The Ormocers® material will stick to the mask from the moment the sample touches the mask

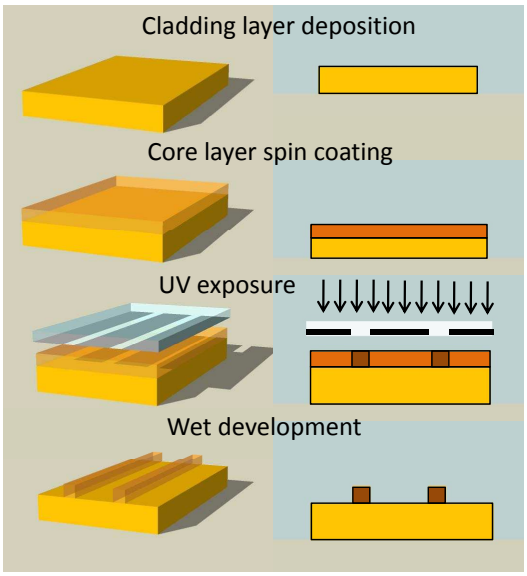

Figure 3.9: Schematic process flow for the fabrication of photolithographic optical waveguides.

and after UV exposure, the layer will even adhere to the glass mask. The material providers admit that non-contact UV exposure is the only solution. The mask aligner set used at CMST does not have a feature to control the z-distance between the mask and the substrate in a repetitive way. A rotating wheel will lower or higher the mask with respect to the substrate, but it is not possible to bring both in satisfying proximity mode. When the mask gets too close to the substrate, they will touch at a certain corner since the parallellism of the two cannot be guaranteed. The FR4-board and the contamination of its sides by previous cured layers will hinder this parallellism. When respecting a certain distance, mask-substrate contacting can be avoided but the resolution of the UV-exposed features is deteriorated. Every result on Ormocers® waveguides in this research is done in proximity mode as a work intensive best effort but has poor reproducibility on the mask aligner at CMST.

waveguide profile

The cross-sectional shape of a waveguide is determined by the material properties and by the UV exposure step. Figure 3.11 gives an overview of the cross-sections of 40 x 50 μm ^{2} waveguides (pitch 250 μm) for the 4 investigated materials applying a 20s, 40s and 60s UV exposure period. The lithography mask used for this purpose has 50 μm wide openings for the waveguide projection. One

would expect waveguides with a width of 50 μm . However, the waveguides are always a bit wider than this 50 μm as can be seen in the pictures. The width of every waveguide is included in Figure 3.11. For Truemode™ Backplane Polymer dry film waveguides the waveguide width variation has been measured and shown in Table 3.6.

Table 3.6: Waveguide width variation for Truemode™ Backplane Polymer dry film waveguides fabricated following the optimized process flow in Table 3.8

Truemode™ Backplane Polymer waveguide width variation	
Sample population	12 pcs
Average waveguide width	63.5 μm
Width standard deviation	5.4 μm
Maximum width deviation	11.5 μm

It is clear from Figure 3.11 that the Truemode™ Backplane Polymer and Epocore / Epoclad waveguides are only wider at the top, while the "foot" of the waveguide is perfectly 50 μm . For even higher UV exposure times, we see that the widening is even visible at the bottom of the waveguide. We can conclude that the widening starts at the top and expands to the bottom with longer UV exposure times. This effect is called T-topping. It results from the lateral diffusion of the acid near the surface. UV lights shorter than 350 nm are absorbed strongly at the top surface of the material. Hence, acid is generated by UV, which diffuses laterally on the top surface. The T-topping effect can be avoided by filtering out short wavelengths below 350 nm [7].

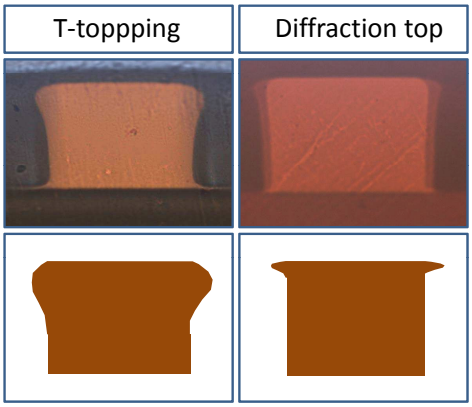

Figure 3.10: Pictures and schematic view of a cross-section from a waveguide suffering from T-topping (left) and a diffraction top (right).

After removal of these short wavelengths, still another effect can be seen at the

very top of the waveguide. This results from the diffraction at the interface between the mask and the material layer and it can be eliminated by filling index-matching oil into the gap. Since this process is quite work intensive and dirty, we will not apply this step in the rest of the work. Figure 3.10 shows photographs and a schematic view of a cross-section from a waveguide suffering from T-topping and a diffraction top. In the cross-sections from Figure 3.11 can be seen that Ormocers® and LightLink™ does not suffer from T-topping effect, although we can see that the waveguide is wider for higher UV exposure times, which can be explained by a general lateral diffusion of acid, which is not concentrated on the waveguide top. Limiting the exposure time or exposure doses can limit this effect to some extent, but a small exposure dose also results in bad adhesion of the waveguides to the undercladding layer. Rinsing of the waveguides after wet development will damage the waveguides if they adhere badly. To ensure good waveguide properties, we chose a medium exposure doses to ensure good adhesion and accept the waveguide dimensions to be wider than 50 μm . The Ormocers® waveguides have a width of 84 μm even for very short exposure times of 20s. This is a result of the non-contact photolithography as depicted in previous section.

The feasibility of smaller pitch parallel waveguide arrays has been investigated. Figure 3.12 gives an overview of the cross-sections of 40 x 50 μm ^{2} waveguides (pitch 125 μm) for the 4 investigated materials applying a 20s, 40s and 60s UV exposure period. Except from the Ormocers® material, 125 μm pitch was no problem to be fabricated. Smaller pitches than 125 μm are not realistic in terms of increasing optical crosstalk between two neighboring waveguide channels.

Waveguide height

The height of a waveguide is only determined by the core layer thickness after spincoating. The spincoating, edge bead removal and layer thickness variation of the core layer are similar to the deposition of the undercladding layer, described in the Section 3.3.2. The core materials need to have a higher refractive index than the cladding material and are thus different in compounding and have thus different spin speed curves and layer thickness variations. Figure 3.13 shows the spin speed curves of the 4 investigated optical core materials, fine tuned around a thickness of about 50μm , which is a waveguide height compatible with standard optical fiber core sizes. Again, the higher viscosity materials need higher spin speeds for the same layer thickness.

The dimensions of the waveguides are even more important than the dimensions of the cladding, since they have a direct impact on the waveguide losses and in- and out-coupling efficiencies. In Figure 3.14, the waveguide heights for 5 different samples for the four materials are shown. Each 5 samples were spincoated right after each other, meaning that the height deviation investigated here, is the

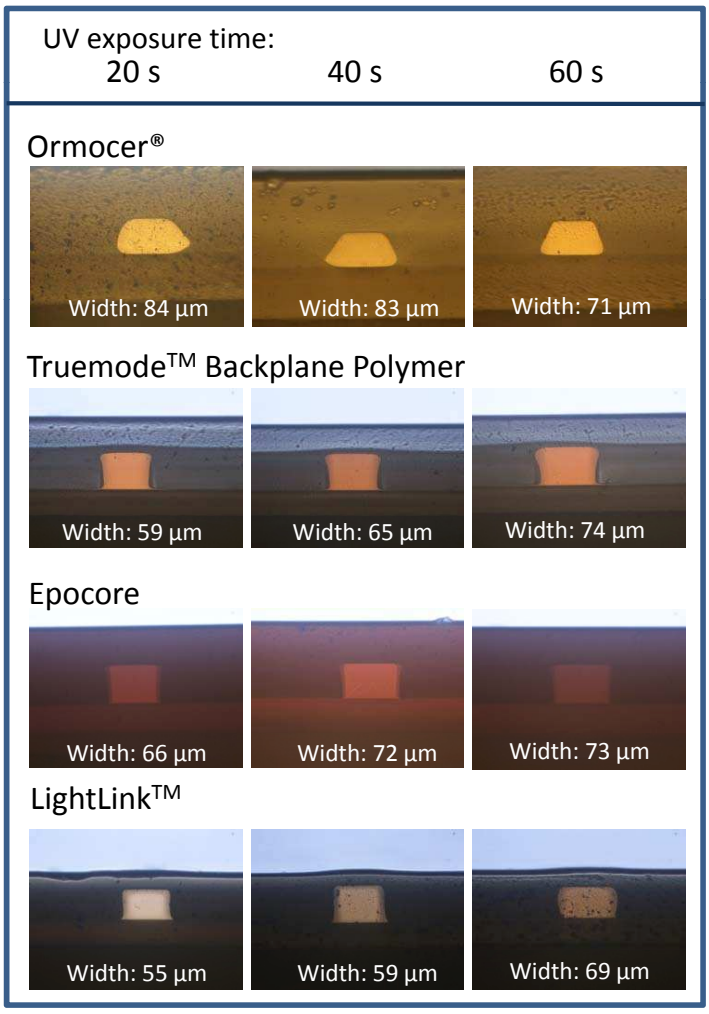

Figure 3.11: Cross-section of 250 μm pitch waveguides in Ormocers® , Truemode™ Backplane Polymer , Epocore / Epoclad and LightLink™ material for different UV exposure times.

short term deviation. It can be seen that LightLink™ shows the highest variation, which can be expected from the very low spin speed of 250 rpm. The spin speed needed to create a 40 μm thick core layer defines to some extend the deviation of the layer thickness. Figure 3.15 shows this spin speed versus the standard deviation of the core layer thickness, which clearly shows that higher spin speeds result in a higher reliable waveguide height. Although it must be said that 5 samples is

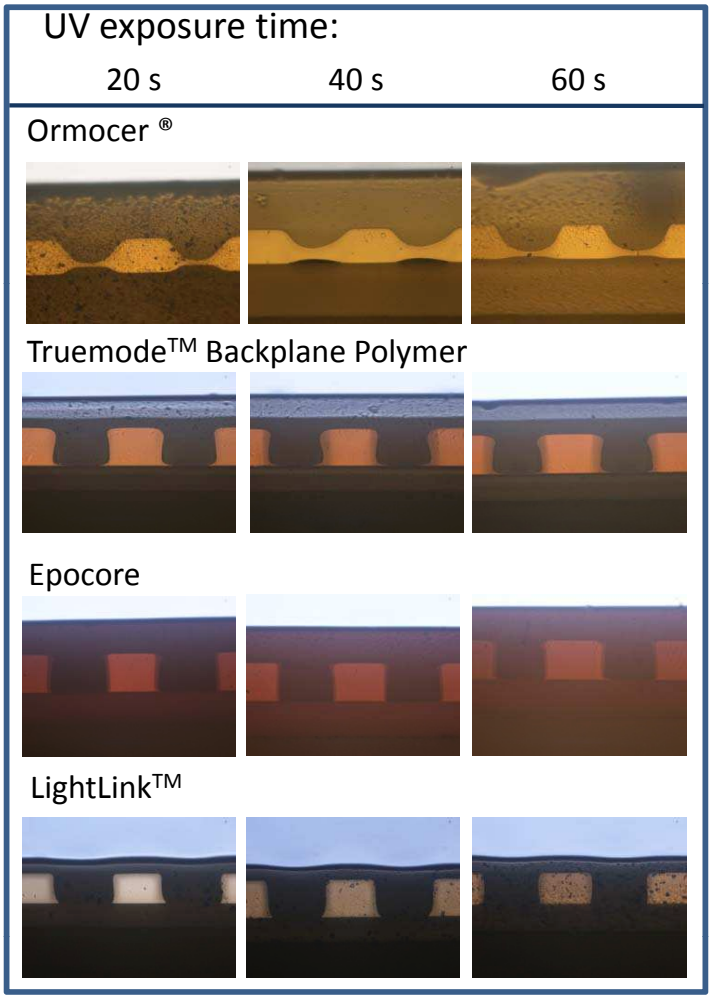

Figure 3.12: Cross-section of 125 μm pitch waveguides in Ormocers® , Truemode™ Backplane Polymer , Epocore / Epoclad and LightLink™ material for different UV exposure times.

not enough to make this theory waterproof.

For Truemode™ Backplane Polymer waveguides, the long term waveguide height deviation was measured (Table 3.7). 12 Samples were measured within a time frame of about 6 months. The maximum thickness deviation of 4.5 μm is acceptable. All these waveguides were made with one batch of Truemode™ Backplane Polymer dry core material. The variation of thickness over multiple

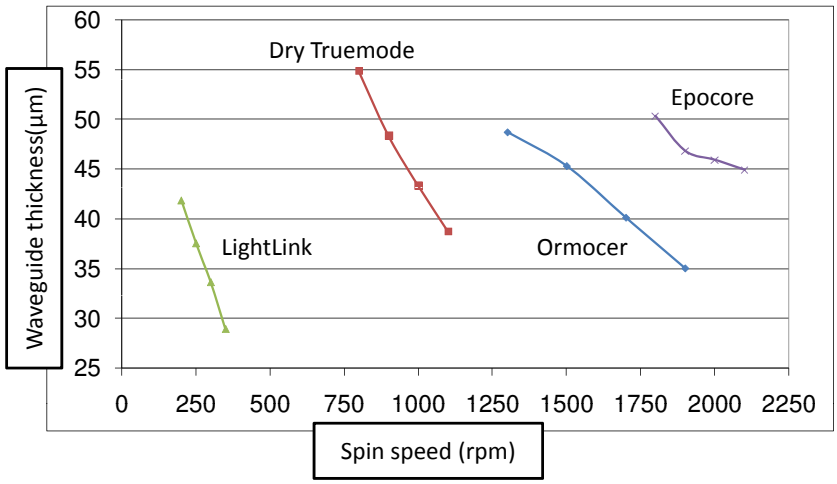

Figure 3.13: Spin speed curves for the core material of LightLink™ , Truemode™ Backplane Polymer , Ormocers® and Epocore / Epoclad .

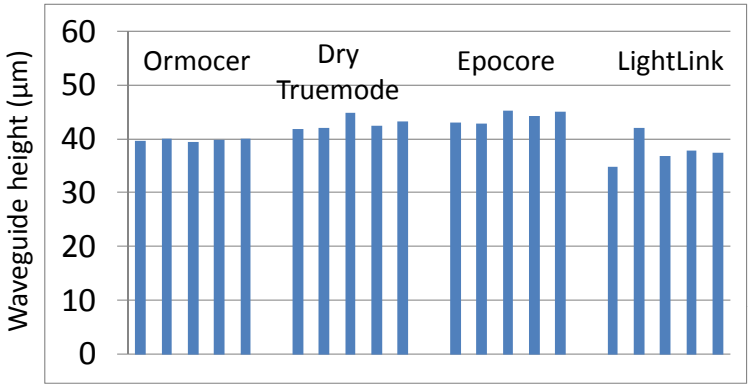

Figure 3.14: Waveguide height deviation for 5 samples of each material.

batches was significant high, meaning that the spin speed adjustment had to be done with every delivered bottle. This is a big disadvantage for the Truemode™ Backplane Polymer material, since we have no idea if the optimized waveguide fabrication parameters will be the same for a next batch.

Table 3.7: Long term Truemode™ Backplane Polymer waveguide height variation

long termTruemode™ Backplane Polymer waveguide thickness deviation (spin speed = 250 rpm)	
Sample population	12 pcs
Average layer thickness	54.5 μm
Thickness standard deviation	2.5 μm
Maximum thickness deviation	4.5 μm

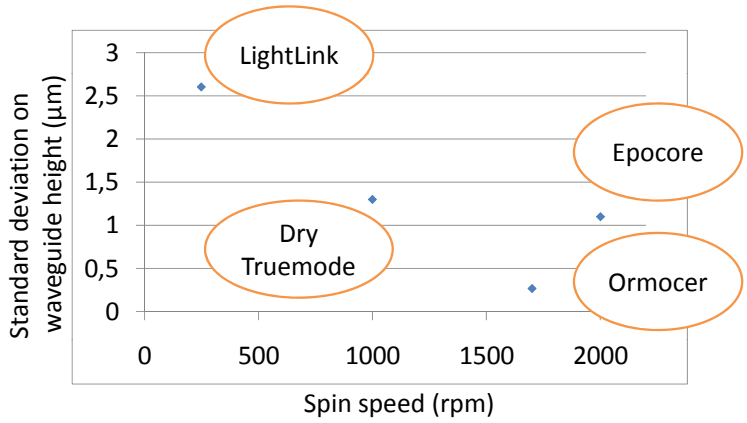

Figure 3.15: Spin speed versus waveguide height deviation for the 4 different materials, aiming at a waveguide thickness of 40μm .

Sidewall roughness

The roughness of the waveguides walls, top and bottom surface have a direct impact on the optical losses of the waveguide. The total waveguide loss has contributions from absorption, intrinsic scattering and extrinsic effects:

$L_{waveguide} = L_{absorption} + L_{scattering} + L_{extrinsic}$
$L_{absorption}$: In polymers, optical losses comes from two main sources: electronic absorption and vibrational absorption. For a wavelength of 850 nm, the most significant contribution comes from the vibrational absorption.
$L_{scattering}$: For a homogeneous material without any structure on the scale of a wavelength of light, the dominant scattering that occurs is Rayleigh scattering.
$L_{extrinsic}$: All optical loss caused by larger scale phenomena as voids, cracks and surface roughness.

This last contribution is completely dependent on the waveguide production process. Macroscopic voids and cracks were never witnessed inside the waveguides

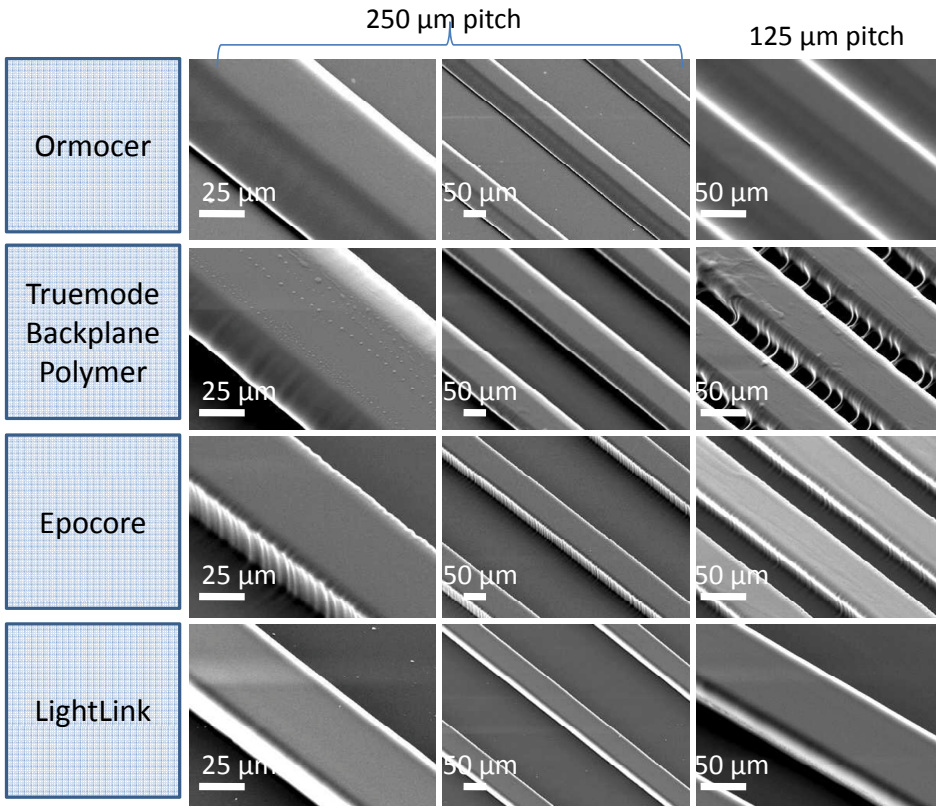

Figure 3.16: Scanning Electron Microscope pictures of Ormocers® , Truemode™ Backplane Polymer , Epocore / Epoclad and LightLink™ waveguides with a pitch of 250 and 125 μm .

when fabricated properly. The surface roughness however is inherent with the photolithographic process. First of all, the edge roughness of the projection mask patterns defines partly the roughness of the side walls, but this mask roughness has been reduced to the minimum by purchasing high quality projection masks. Other factors like diffraction, light absorption, shrinkage, etc. play a role in the formation of the waveguide walls. A detailed characterization of each contributor is out of the scope of this work and has been done by others in the past [8, 9, 10, 11]. We will limit ourselves in this study to the measurement of the waveguide sidewall roughness. Figure 3.16 shows scanning electron microscope (SEM) images of waveguides in the four investigated materials applying a 60s UV exposure time. The samples were coated with a flash of carbon to prevent static electrical loading of the sample during SEM photography. 250 μm and 125

μm pitch waveguides are shown. The Truemode™ Backplane Polymer and especially the Epocore / Epoclad waveguides show ridged side walls which will result in higher optical losses. The LightLink™ waveguides looks best on these SEM pictures. Something which could not be seen in the cross-sectional waveguide views is that the 125 μm pitch Truemode™ Backplane Polymer waveguides show sidestrings in between two neighboring waveguides, which is also disadvantageous for the optical loss. Fine tuning of the UV exposure time could solve this problem.

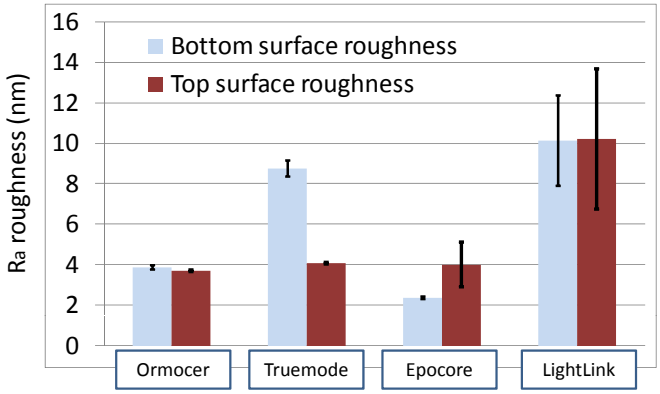

Figure 3.17: Ra roughness of waveguide top and bottom surfaces. Waveguides were fabricated in Ormocers® , Truemode™ Backplane Polymer , Epocore / Epoclad and LightLink™ . WYKO non-contact profilometer measurement on an area of 50 x 50 μm ^{2}

Figure 3.17 shows the roughness of the top and bottom surface of the waveguide for the 4 investigated materials together with the standard deviation, measured over 5 different measurements. The measurement area was 50 x 50 μm ^{2}. This is actually the roughness of the spin coated surfaces of respectively the undercladding and the core layer and is expected to be low due to the properties of the spincoating process. The highest value was found for the LightLink™ material, but the roughness is still much smaller than 10% of the datacom wavelength (850 nm). This is considered as a rule of thumb to define if certain features will influence the optical path and thus cause extra optical losses.

Figure 3.18 shows the roughness of the side walls of the waveguide measured on an area of 15 (height) x 30 (length) μm ^{2} which we will define as the sidewall curvature measurement and on an area of 5 x 5 μm ^{2} which we will define as the micro-roughness measurement.

To be able to do this measurement, the substrate was cut right next to the waveguide. The waveguides were protected from dust during the cutting by applying a

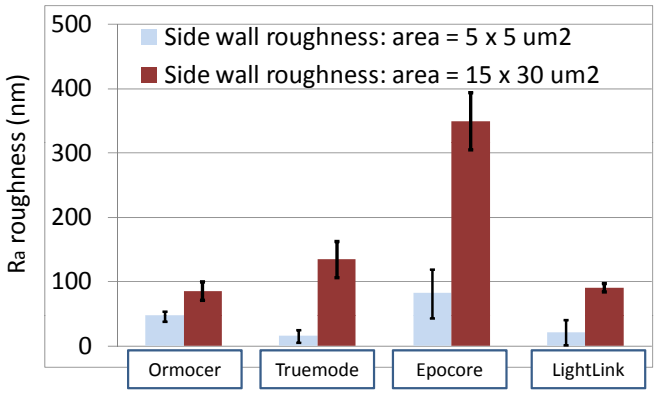

Figure 3.18: Ra roughness of waveguide side wall surfaces. Waveguides were fabricated in Ormocers® , Truemode™ Backplane Polymer , Epocore / Epoclad and LightLink™ . WYKO non-contact profilometer measurement on an area of 5 x 5 μm ^{2} and on an area of 15 x 30 μm ^{2}.

sacrificial photoresist layer on top of the waveguides before cutting, which is then removed afterwards. Again a carbon flash coating was provided for a good measurement since non contact profilometry on a transparent layer is a very hard job. The measurements show that the micro-roughness is acceptable for all materials except for Epocore / Epoclad . The sidewall curvature measurement is of course much higher, especially for the Epocore / Epoclad which will suffer from much higher optical losses. The reason for the extreme ridged sidewalls of Epocore / Epoclad waveguides is not clear, further research should be done to find the reason and thus solve this issue. The sidewall curvature of Truemode™ Backplane Polymer is slightly above the 10%-of-wavelength level, but is acceptable for short distance communication channels. For the micro-roughness measurements, the tilt and cylindrical terms were removed from the measurement data to obtain the real nominal roughness.

A plot of one of the WYKO measurements for each waveguide material for top, bottom and side wall is included in Figure 3.19. The plots give a good qualitative comparison of the different materials, but one must take into account that each plot has a different surface height scale. The top surface Truemode™ Backplane Polymer roughness plot shows circular non-uniformities. These are actually residue drops from the development of the sacrificial photoresist layer, which

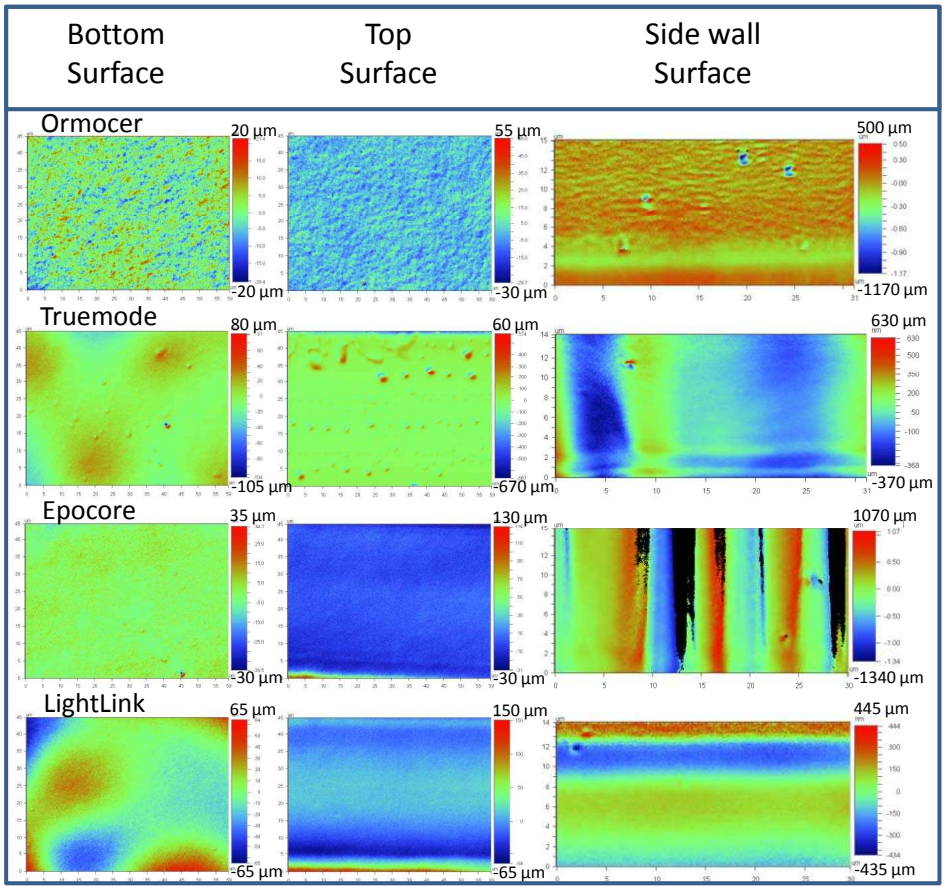

Figure 3.19: WYKO non-contact profilometer plot of Ra roughness measurements on the top and bottom surface of waveguides in Ormocers® , Truemode™ Backplane Polymer , Epocore / Epoclad and LightLink™ material (50 x 50 μm ^{2} area) and on the side wall surface (15 x 30 μm ^{2} area).

was applied on waveguides to do the cross-section. These residues are not representative and should be ignored. The black areas in the side wall plot of Epocore / Epoclad waveguides are areas were no measurement values could be taken, because the surface was too steep or not coated with carbon. We can assume that the side wall roughness value will be a bit higher than the measured value shown in Table 3.18.

Table 3.8 shows the optimized process flows for the core layer for Epocore / Epoclad , Ormocers® , Truemode™ Backplane Polymer and LightLink™ for

Table 3.8: Optimized process flows for the core layer for Epocore / Epoclad , Ormocers® , Truemode™ Backplane Polymer and LightLink™ for aimed cross-sectional dimensions of 50 x 50 μm ^{2}.

Epocore / Epoclad core layer process flow	
Process step	Process parameters
Spin coat	1800 rpm
Prebake hotplate	45 min. ; 85 ^{o}C
UV exposure	20 s ; 10 mW/cm^2
Post exposure bake hotplate	15 min. ; 50 ^{o}C
	and 10 min. ; 85 ^{o}C
Wet developing	60 s ; MrDev600
Rinse	IPA
Dry	N_2
Hard bake	60 min. ; 150 ^{o}C
Ormocers® core layer process flow	
Spin coat	1300 rpm
Prebake hotplate	NO prebake !
UV exposure	60 s ; 10 mW/cm^2
Post exposure bake hotplate	10 min. ; 85 ^{o}C
Wet developing	20 s ; Ormodev
Rinse	IPA
Dry	N_2
Hard bake	60 min. ; 150 ^{o}C
Truemode™ Backplane Polymer core layer process flow	
Spin coat	900 rpm
Prebake hotplate	2 min. ; 95 ^{o}C
UV exposure	20 s ; 10 mW/cm^2
Post exposure bake hotplate	3 min. ; 110 ^{o}C
	10 min. ; 125 ^{o}C
Wet developing	4 min. ; MrDev600
Rinse	IPA
Dry	N_2
Hard bake	60 min. ; 150 ^{o}C
LightLink™ core layer process flow	
Spin coat	200 rpm
Prebake hotplate	30 min. ; 90 ^{o}C
UV exposure	40 s ; 10 mW/cm^2
Post exposure bake hotplate	3 min. ; 90 ^{o}C
Wet developing	40 s ; OptodevXP
Hard bake	60 min. ; 150 ^{o}C

aimed cross-sectional dimensions of 50 x 50 μm ^{2}.

3.3.4 Uppercladding layer

layer deposition

The uppercladding layers need to cover the waveguide completely to fulfill complete embedding of the waveguides. The uppercladding layer needs to have the double thickness of the undercladding or core layer because it not only has to fill the gap in between the waveguides, but has to cover them on the top as well with a sufficient thickness. Figure 3.20 shows this schematically. For Truemode™ Backplane Polymer and LightLink™ material, the low viscosity of the material restricts the total spin coatable layer thickness to about 35 μm. The uppercladding layer must be applied in two consecutive steps. The uppercladding for Ormocers® and Epocore / Epoclad can be applied in one single step.

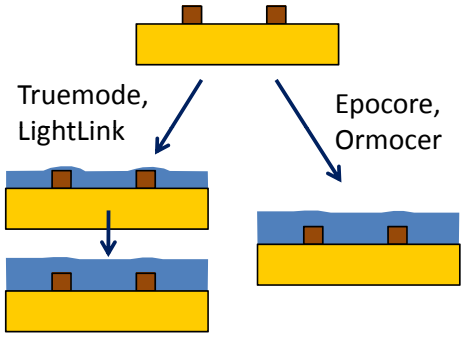

Figure 3.20: Applying of the uppercladding layer to cover the waveguides for Truemode™ Backplane Polymer , LightLink™ , Ormocers® and Epocore / Epoclad

When applying fluid material over irregular surfaces as waveguides, the risk for encapsulated air bubbles is real. A good method to avoid this, is to apply the material in the middle of the waveguides, and tilt the substrate in all directions manually. This way the material will slowly be spread over the waveguides and the rest of the substrate, pushing the air forward instead of encapsulation it. When the material is spread all over the substrate, the material will not create air bubbles anymore during the spinning.

Uppercladding thickness

The thickness of the uppercladding is difficult to define, because perfect planarization is not realistic. The thickness of the uppercladding layer is more a

distribution. Since this layer is often the last layer to be applied, its planarization is of minor importance. The laser ablation of micro mirrors through the uppercladding and the core layer, later on in this research, demands however that the uppercladding thickness is controllable or at least reproducible. During first trials it was clear that something needed to be done to answer this demand. When spincoating an uppercladding layer on top of a waveguide array of 12 waveguides with a pitch of 250 μm , the difference between the uppercladding thickness on top of the middle waveguide and on the edge waveguide could rise up to 20 μm for LightLink™ waveguides.

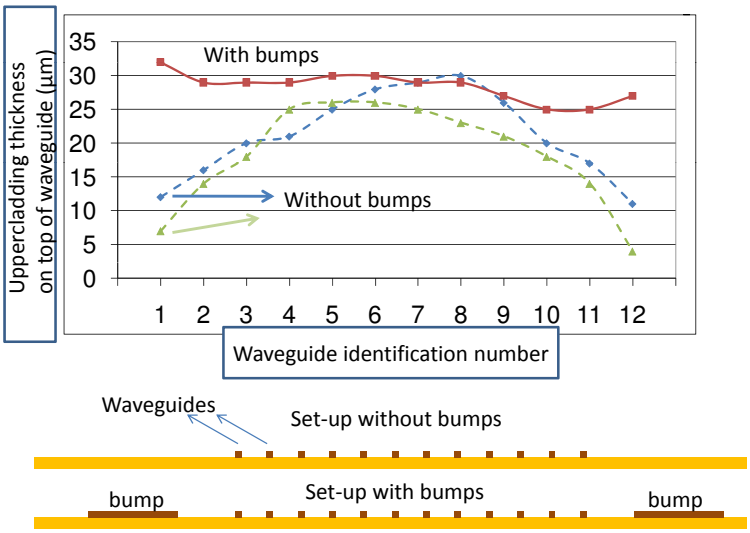

Figure 3.21: Schematic sketch of the bump principle for the reproducibility of the uppercladding thickness on top of the waveguides (bottom) and the uppercladding thickness for 12 different waveguides in a 1 x 12 waveguide array for bumped and non-bumped waveguide fabrication (top).

The introduction of bumps can solve this problem. Figure 3.21 explains the principle of the bumps and shows the thickness of the uppercladding layers on top a each waveguide of the waveguide array. The bumps are actually non-functional wide waveguides, fabricated in the same process step as the other waveguides. We see that the maximum deviation of the uppercladding thickness on top of the waveguides is reduced to 4 μm , which is a more acceptable value. Without bumping, the uppercladding thickness on the outer waveguides can even be below 5 μm . This is unacceptable. The uppercladding layer must be at least 25 μm thick to ensure good light propagation functionalities.

The introduction of bumps enlarges the total footprint of the waveguide ar-

ray. However this is just limited, since the bumps don't need be scaled with the amount of waveguides in the waveguide array. In other words, whether the waveguide array consists of 4 waveguides or 20 waveguides, the amount of bumps is the same.

The variation on the thickness of the uppercladding far away from the waveguides (1cm distance) over multiple substrates for Truemode™ Backplane Polymer waveguides is shown in Table 3.9. The maximum deviation of 11 μm is about the double of the maximum deviation for the spin coating of one single layer on a flat substrates.

Table 3.9: Variation on the thickness of the uppercladding layer over multiple samples.

long termTruemode™ Backplane Polymer uppercladding thickness variation (spin speed = 250 rpm); double layer deposition	
Sample population	11 pcs
Average layer thickness	62 μm
Thickness standard deviation	5 μm
Maximum thickness deviation	11 μm

Table 3.10 shows the optimized process flows for the uppercladding layer for Epocore / Epoclad , Ormocers® , Truemode™ Backplane Polymer and LightLink™ for aimed thickness of 50 μm on top of the waveguides.

Table 3.10: Optimized process flows for the uppercladding layer for Epocore / Epoclad , Ormocers® , Truemode™ Backplane Polymer and LightLink™ for aimed thickness of 50 μm on top of the waveguides.

Epocore / Epoclad core layer process flow	
Process step	Process parameters
Spin coat	1500 rpm
Prebake hotplate	60 min. ; 85 ^{o}C
UV exposure	120 s ; 10 mW/cm^2
Post exposure bake hotplate	15 min. ; 85 ^{o}C
Hard bake	60 min. ; 150 ^{o}C
Ormocers® core layer process flow	
Spin coat	750 rpm
Prebake hotplate	5 min. ; 85^{o}C
UV exposure	120 s ; 10 mW/cm^2
Post exposure bake hotplate	5 min. ; 85 ^{o}C
Hard bake	60 min. ; 150 ^{o}C
Wet developing	20 s ; Ormodev
Rinse	IPA
Dry	N_2
Truemode™ Backplane Polymer core layer process flow	
Spin coat	250 rpm
UV exposure	60 s in $N_2 environment$; 10 mW/cm^2
Spin coat	250 rpm
UV exposure	60 s in $N_2 environment$; 10 mW/cm^2
Hard bake	60 min. ; 150 ^{o}C
LightLink™ core layer process flow	
Spin coat	250 rpm
Prebake hotplate	20 min. ; 90 ^{o}C
UV exposure	120 s ; 10 mW/cm^2
Post exposure bake hotplate	10 min. ; 90 ^{o}C
Spin coat	250 rpm
Prebake hotplate	20 min. ; 90 ^{o}C
UV exposure	120 s ; 10 mW/cm^2
Post exposure bake hotplate	10 min. ; 90 ^{o}C
Hard bake	60 min. ; 150 ^{o}C

3.4 Conclusions

The different waveguide fabrication method possibilities are discussed shortly and compared with respect to their use in the fabrication of flexible waveguides. Within the presented research, the choice was made to use standard photolithography. This process was studied in more detail. The process flows for the creation of waveguides in Truemode™ Backplane Polymer , LightLink™ , Epocore / Epoclad and Ormocers® was optimized in function of waveguide profile, waveguide roughness and dimensions. An analysis of dimensional short term and long term variations was made in the scope of embedding active components and coupling elements later on in the research, were positioning requirements become very strict. Especially planarization of the different spincoated materials was characterized. Process problems like edge bead, adhesion issues, air bubble insertions, proximity mode UV exposure and waveguide T-topping were studied and tackled within the possibilities.

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Chapter 4

Flexible optical waveguide foil

This chapter takes the principle of optical polymer waveguides on board to another dimension. The waveguide stack developed and described in chapter 3, will be adjusted to allow the waveguides to be bent. Polyimide support layers offer the necessary strength and support for the poorly flexible optical waveguide materials. This chapter describes the efforts to integrate the optical waveguide stack on top of a Polyimide foil, in between two spincoated Polyimide layers and laminated between two Polyimide foils.

4.1 Introduction

At the start of this research, flexible optical commercially available polymers were lacking. Most of the todays existing flexible optical waveguide polymers where developed in the past 4 years and are barely commercially available (see Chapter 2). Exceptions to this are silicones and polyimide materials, but these materials lack processability. This gets more significant further in this work, where the embedding of actives and light coupling components is introduced.

The work described in this chapter tackles this issue by exploring the flexibility of the materials which were developed for the use on rigid boards. Support layers can improve the mechanical behavior significantly and can push the existing non-flexible materials into the flexible material categories.
Using flexible materials which are optimized for bending is still the best choice with respect to mechanical behavior but with respect to cost, using the established optical materials is the right choice for now.

Lamination of polymer waveguides on or between mechanical support layers to realize an alone-standing waveguide foil isn't a new concept:

- People of the Optics and Photonics Elite Research Academy (OPERA) of the Inha University of Korea developed their own optical waveguide material for rigid substrates and dared to apply them on a flexible PET foil with very good results. Bending radii down to 2 mm were feasible [1].

- The University of Dortmund laminated waveguides of commercially available material from Wacker Chemie, Burghausen, Germany in between different laminates. They found a relationship between the laminate material and the thermal stability of the laminated waveguides. Figure 4.1 shows the optical loss of 70 x 70 μm ^{2} cross-sectional waveguides after temperature treatment upto 300 ^{o}C with different laminate materials.

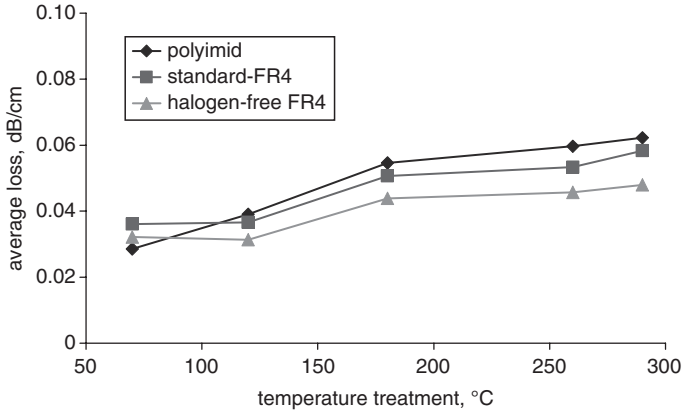

Figure 4.1: Thermal stability of waveguide foils transmission loss @ 850 nm using different PCB laminates. (source: University of Dortmund).

They also noticed that the optical losses of the waveguides increased significantly after the 260 ^{o}C solder reflow temperature test when the FR4 was used as a laminate. This is caused by the outgassing of the flame retarding constituents from the FR4 which can diffuse into the highly expanded waveguide material. Polyimide does not show this effect [2].

- Researchers at the Korea Photonics Technology Institute developed a flexible optical waveguide link made of Epoxy material. A 10 μm thick Polyimide is provided on the undercladding layer to protect the layer and for mechanical support [3]. The use of Polyimide is attractive to implement electrical interconnection on this support layers. They brought this aspect into practice.

- The University of Loughborough, England, did a study on the effect of surface modification on adhesion of polymer waveguides on flexible substrates

and on the role of chemical interaction and interfacial characteristics on the optical properties of the waveguides [4].

- The company Optical Crosslinks sells finished flexible waveguide foils, fabricated with their own patented fabrication method. Their waveguide stacks are all provided of an outer jacketing layer of Aralite or Kapton with a SiO_x layer to block moisture penetration [5].

- The University of Texas at Austin used Topas^{TM} foils from Ticona first as undercladding layer for their flexible waveguide layers [6] and later on purely as support layers [7].

- The Georgia Institute of Technology in Atlanta, USA [8] and the Electronics and Telecommunications Research Institute in Korea [9] also used a Polyimide foil as sandwich carrier material for its flexible optical waveguides.

4.2 The principle of the neutral axis and supporting layers

The enhancement of the flexibility of a waveguide stack is based on the principle of the neutral axis and the use of supporting layers . When bending a material with a Young's modulus E over a bending radius R, strain (ϵ) will be induced inside this material. The "outside" surface will feel a tensile strain and the "inside" surface will feel a compressive strain. The stress (σ) inside the material due to this strain will be a distribution inside the material which is linear to the lateral distance to the longitudinal axis of the material. The formula for this stress is depicted in Figure 4.2 together with the schematic overview of this principle. The material layer on the longitudinal axis will feel zero stress. This is why we call this axis the neutral axis. The highest stresses in the waveguide stack can be found in the outer layer. Different build-ups of Polyimide and optical layers are investigated and described in the following sections. As explained in the schematic Figure 4.2, the maximum stress in the optical layers is reduced significantly if the layers are in the center of the layer build-up, as close to the neutral axis as possible.

By applying layers of Polyimide on both sides of the stack as physical supporting layers, we can spread the high stress inside the outer optical polymer over a larger area than just the bending area. Polyimide has a high strength and flexibility which makes it the ideal support material.

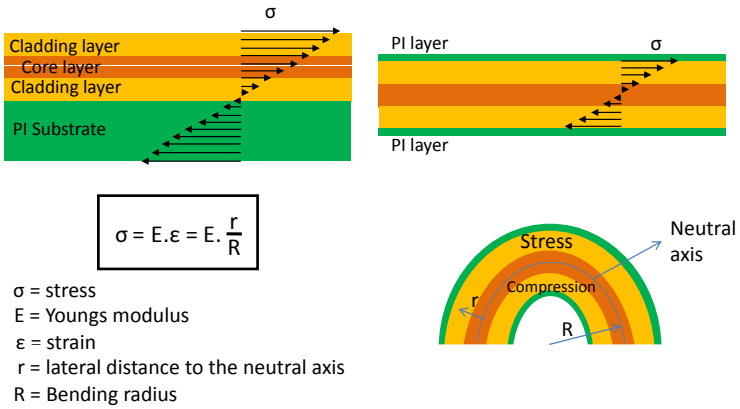

Figure 4.2: Principle of the neutral axis executed on the waveguide stack.

4.3 Coefficient of thermal expansion (CTE) considerations

By laminating the optical layers between support layers, we provide a jacketing layer build-up. This way a free standing waveguide film with mechanical stability at elevated temperatures can be realized. The difference in Coefficient of thermal expansion (CTE) plays a very important role in this stability. Adhesion of the polymer to the substrate is a major failure concern. Stresses are created at the polymer/substrate interface due to differences in the CTE between the two materials. These stresses can be large at room temperature due to the high processing temperature required to cure the polymers: the processing temperatures can be higher than 200 ^{o}C for Polyimide . The amount of stress is proportional to the CTE mismatch and the polymer film thickness [10]. If the stress is greater than the adhesion strength of the polymer/substrate interface, the polymer will delaminate from the substrate. Stress cracks at features corners like via holes are another potential problem since the cracks tend to grow with thermal cycling. Optimization of the processing steps can minimize this effect [11]. Even if the Polyimide does not delaminate from the substrate or base material, the stress may cause the substrate to warp. As a rule of thumb, the thickness of a temporary rigid carrier substrate should be 20 times the thickness of the Polyimide to avoid this [12].

The packaging layer essentially determines the effective CTE and Tg of the complete waveguide foil:
For example: When the flexible waveguides of Optical Crosslinks [5] are pack-

aged within Kapton layers which have a CTE of around 20 ppm and a Tg near 350^{o}C, the effective waveguide foil CTE is 25 ppm. Kapton packaging enables process stability under standard 230^{o}C thermal shock. When Polycarbonate with a CTE of 70 ppm and a Tg near 150^{o}C is used, the effective waveguide CTE will be identical to that of the Polycarbonate. In addition, the packaged structure is stable upto 155^{o}C.

The support Polyimide layers and investigated optical layer CTE's are shown in Table 4.1. The PI2525 series should show best results due to its proximity in CTE value. This is proven to be true later on in this Chapter.

Table 4.1: Coefficient of Thermal Expansion (CTE) for different Polyimide materials and optical polymers.

Polyimide materials			
Material type	material name	provider	CTE (ppm/K)
Foil	Upilex S-25	UBE America Inc. [13]	12
Spincoatable resin	PI-2611	HD Microsystems [14]	3
Spincoatable resin	PI-2525	HD Microsystems [14]	40
Optical waveguide materials			
Material		provider	CTE (ppm/K)
Truemode™ Backplane Polymer		Exxelis Ltd. [15]	60
Ormocers®		Micro resist [16]	100-130
Epocore / Epoclad		Micro resist [16]	50
LightLink™		Rohm and Haas [17]	unknown

4.4 Lamination of optical waveguide layers

To provide a waveguide stack with support layers, three approaches are possible: lamination between two supporting foils, direct processing of the waveguide stack on a foil and processing of the supporting layers in one process with the waveguide layers.

Lamination of an optical waveguide stack between Polyimide layers consists of the stacking of a bottom Polyimide foil, the optical waveguide stack and a top Polyimide foil with an adhesive layer in between every layer. This layer stack can then be pressed together with controlled pressure and heat to reflow and cure the adhesive layers. The lamination technique has been reported several times, each with success.

4.4.1 Waveguide stack release

To make use of the lamination principle, we must be able to fabricate a stand-alone waveguide stack. The processing needs to be done on a temporary rigid carrier to achieve compatibility with standard existing PCB manufacture equipment. This means we need a kind of release method which allows processing on a rigid carrier and which can release the stack afterwards. A release method would need to fulfill following requirements:

- The release layer must be able to be solved in a solvent after processing, loose its adhesion strength with respect to the waveguide stack material or be able to be peeled off.
- If the layer is a dissolvable type, the solvents for releasing should not degrade the optical stack
- The release layers needs to withstand temperatures up to 150 ^{o}C for several hours, which occurs during the waveguide stack processing.
- The spincoated waveguide undercladding layer should not interact with the release layer.
- The release layer must not be affected by the chemicals used during processing of the waveguide stack (acetone, IPA, wet developers, water).

Several methods were investigated with little satisfying results. The release methods can be separated in four types: dissolvable layers, heat releasing layers, UV releasing layers and peel off layers.

Dissolvable release layers

- Spincoated wax layers: commercially available wax is often used to temporary bond foils to a rigid substrate but the melting temperatures of the available waxes are not high enough to stay hard during the curing cycles of the optical waveguides.
- Photoresist AZ4562 [18] is used often as lift-off layer for the patterning of Ag metallization layers. The photoresist was cured @ 120 ^{o}C before the spincoating of the optical layers. Stripping of the resist underneath the optical layers is a problem, even after several hours of bathing inside photoresist developer and stripper, the layer is not etched away.
- Prolift^{TM} 100 from Brewer Science [19] is developed as a release layer for MEMS processing. Same problem occurs: The etching of the release layer will not happen underneath a complete 2 by 2 square inch layer.

- Cryolite (sodium hexafluoroaluminate), KCl (potassium chloride) and NaCl (kitchen salt) can be evaporated onto the substrate and can be dissolved at the end of the processing with water. Problem is that water is present in the air and slowly penetrates into the layers which results in the early release of the optical material. Any further processing from that point is not possible.

- Water soluble cellulose used as package material for medicines is again water soluble and the highest melt temperatures are still too low.

- PVA (polyvinylalcohol) works very fine as a release layer for PDMS. Spinning optical layers on this PVA however results in a reaction between spin-coated optical polymer and the PVA. The release is also water-based.

- Copper coated FR4 is a possible candidate. After processing of the waveguide stack on top of the copper layer, this latter can be etched away with copper etchants. Copper etchants do not contaminate the investigated optical materials. This technique however has the disadvantage that thin layers will curl up during release. Figure 4.3 shows a picture of a partly released single Ormocers® layer by stopping the copper etch after 15 minutes. The layer curls up due to its low stiffness.

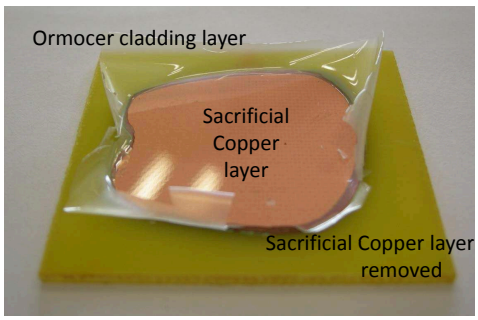

Figure 4.3: Partly released Ormocers® cladding layer processed on a copper coated FR4 board.

The release of thicker layers, like a complete undercladding / core / upper-cladding also shows slight curling of the layers but not in such an extent that further processing is impossible.

Heat releasing layers

Commercially available heat releasing adhesives will adhere very well to the substrate and the optical polymers until a certain temperature is reached, at which

point, the adhesion will be lost and the polymer will release. However the highest release temperatures for this kind of adhesives are still too low. The answer to the request to a technical support engineer of Nitto Denko, one of the world largest tape providers, for a tape which can fulfill all the requirements named above, the answer is that a tape with the required characteristics is not available at all in the market today.

UV releasing layers

UV release layers are developed to pick and place diced wafers. After dicing of the wafers, the single dies stick to the adhesive tape. A single local UV exposure can release the dies from the tape very easily. UV exposure is however an essential process step during the fabrication of the optical waveguide, so the use of this kind of release is out of the question.

Peel off layers

Peel off release is the most common method in literature for the creation of flexible waveguide films. The layers are processed on a flexible sacrificial film, which is often chemically treated to ensure peel-off. The foil must have just enough adhesion to hold the processed layers during the different process steps but not too much adhesion to be able to be peeled off afterwards. This is a quite critical issue. The harsher the process steps are, the higher demands for the peel-off layers. Optical Crosslinks [5] fabricates optical waveguide foils with a roll-to-roll process using a peel-off technique. However they use dry film precoated undercladding layers and cure temperatures no higher than 45 ^{o}C. The photolithographic process we use needs much higher temperatures, resulting in higher CTE difference importance, more curing shrinkage, etc. Another major drawback in our process is the fact that the spincoated materials are not flexible and strong but rather brittle as an alone-standing layer, meaning that peel-off often results in breakage of the layer stack.
The peel-off technique has been tried for the 4 investigated optical materials on three different peel-off set-ups. Figure 4.4 shows the schematic overview of these three techniques.

- Direct processing of the optical polymer layers on top of a foil has some limitations for peel-off: the foil needs to be quite thick, otherwise the material is not stiff enough for spincoating. However, the stiffer the foil, the trickier is the peeling off. During peel-off, the substrate or the optical polymer needs to be bent. In case of a stiff Teflon layer, most of the bending has to been done by the polymer which is too brittle. This technique has been tried out with Teflon foil. Other foils covered with a sprayed Teflon layer resulted in the contraction of the optical material on top of this sprayed Teflon layer.

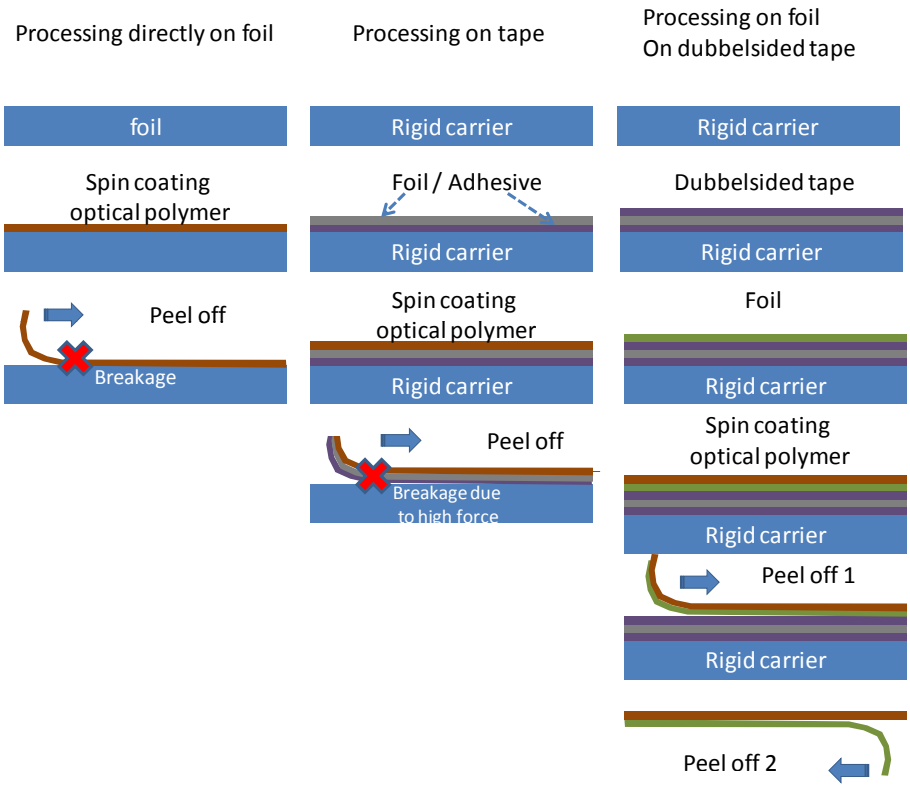

Figure 4.4: Peel off techniques for the release of optical polymer stacks after processing on a temporary rigid substrate.

- Different tapes, consisting of foil with an adhesive coating at the backside were tried out, but after curing temperature of 150 ^{o}C, these tapes adhere too well to the temporary rigid substrate. A high pulling force is needed to peel off the tape from the temporary rigid carrier. This high force results in breakage of the optical polymer layers.
- The only good results were obtained by combining tapes and foils to be used as a double peel-off technique. A doublesided tape is mounted on top of a ceramic substrate. This doublesided tape consists of a foil coated at both sides with an adhesive. One side has a strong adhesive and one side has a weak adhesive layer. The hard adhesive side is mounted downwards on the ceramic substrate. On the weak adhesive side (upwards), another foil is mounted. After spincoating of the polymer optical layers, the latter foil + optical layers are peeled off together. Since the upper adhesive side

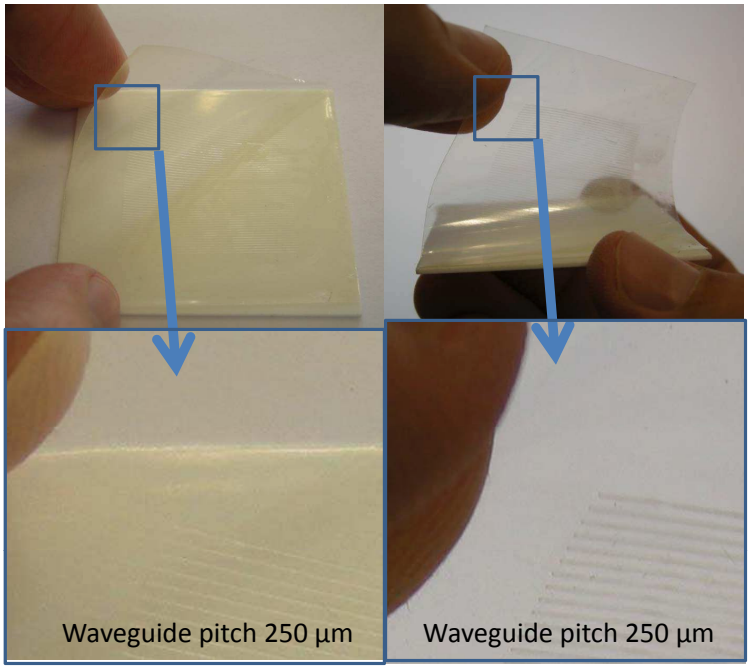

Figure 4.5: Manual release of a completed Epocore / Epoclad waveguide stack using the doublesided tape and LF0100 foil.

of the doublesided tape has weak adhesive, this can be done by applying low peel-off force. The optical layers do not break due to the support given from the upper foil. Afterwards this foil can be peeled off from the optical layer by only bending the foil and not the optical layers, so they stay intact. The foil used for this technique needs to show low hydrofility to realize the spincoating without contraction of the optical material and needs to show low adhesion to the optical polymer after the complete processing, including the hardbake. Different available foils were tested for this issue and only one reached the requirements: Pyralux LF0100 from Dupont [20]. It is a 25 μm thick C-staged modified acrylic adhesive sheet. The primary use for this adhesive is to bond flexible inner layers or rigid cap layers in multilayer lamination. It is also widely used to bond flexible circuits to rigid boards during the fabrication of rigid-flex circuits, as well as to bond stiffeners and heat sinks. Figure 4.5 shows the manual release of a completed Epocore / Epoclad waveguide stack using the doublesided tape and LF0100 foil. The doublesided tape is the REVALPHA tape from Nitto Denko [21].

4.4.2 Lamination process

A released waveguide stack in Truemode™ Backplane Polymer , Ormocers® , Epocore / Epoclad or LightLink™ is too brittle as stand-alone layer. After release, this stack is laminated in between two Polyimide UPILEX S-25 foils from UBE America Inc. [13], using a B-stage acrylic adhesive. This is done with a basic dry film roll laminator from MegaElectronics UK [22] (see Figure 4.6 (left)). The principle is very simple (see Figure 4.6 (right)). The stack of dry films Polyimide /adhesive/waveguide-stack/adhesive/Polyimide is pressed together with controlled pressure between two rotating, heated rolls. The working temperature was 130 ^{o}C to fully cure the adhesive layers. The rotation speed was chosen to be as low as possible to prevent air bubble insertions.

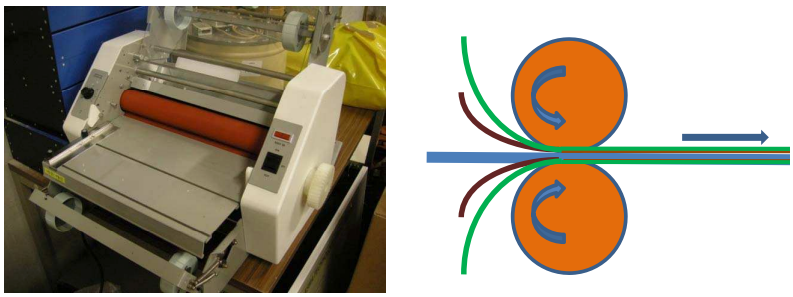

Figure 4.6: Dry film laminator picture (left) and schematic principle of the lamination process (right).

Cross-sectional pictures of laminated waveguide stacks are shown in Figure 4.7. After lamination, the adhesive layer has a thickness of 18 μm , which is very consistent over the whole substrate area. No air bubble insertions are witnessed except at the edges of the waveguide stack. There we see air bubble insertions and double folding of the adhesive as depicted in the bottom 6 pictures of Figure 4.7. This can be solved with vacuum lamination conditions, but the edges can also be cut out after lamination. This will however result in unprotected waveguide polymer at the edges.

The resulting substrate is shown in Figure 4.8. The final substrate shows great strength due to the strength of the Polyimide foils, but the flexibility is below the expectations. The acrylic adhesive at both sides has a thickness of about 18 μm ; together with the Polyimide foils of 25 μm thickness, the lamination process extends the thickness of the waveguide stack with 86 μm which explains partly the limited flexibility. Flexible adhesive layers are nowadays available on the market, which will increase the flexibility. However the optimization of the lamination process is not within the scope of this work. We aim at a final substrate which is as thin as possible as part of the idea of miniaturization. Lamination is a mature

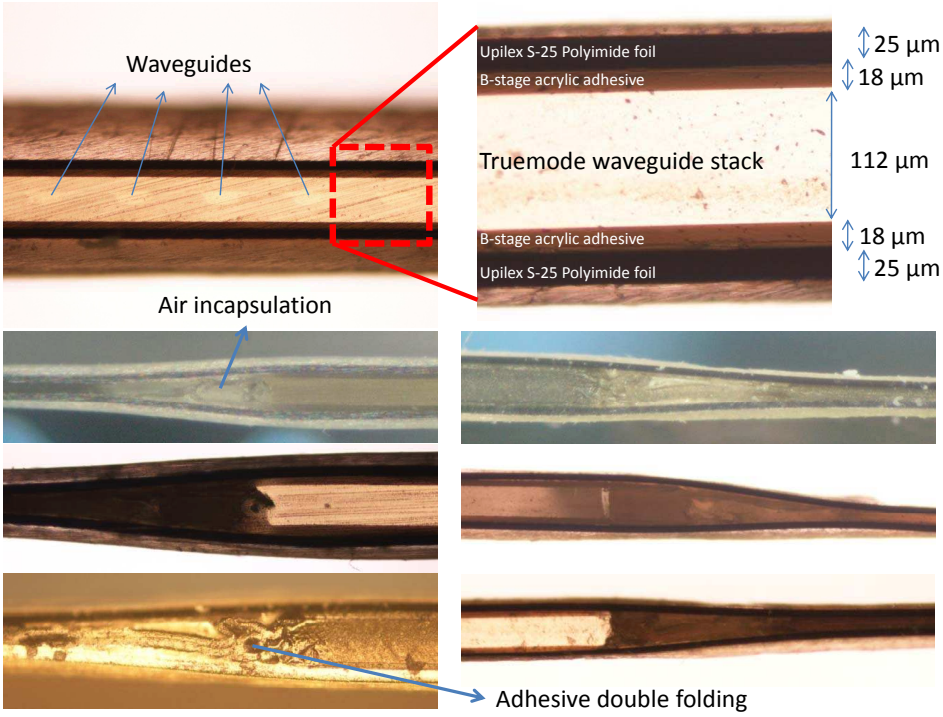

Figure 4.7: Cross-sections of a Truemode™ Backplane Polymer laminated waveguide stack with the layer thicknesses (top 2 pictures) and close-ups on the edges of the waveguide stacks (bottom 6 pictures)

process and used on large scale electronics, so further research on this would not be an additional value to the state-of-the-art technology and know-how.

4.5 Waveguide stacking on Polyimide foil

The starting approach for the fabrication of flexible waveguides was the processing of the waveguide layers directly on top of a flexible foil. As will be described in this section, this did never show good results.
The following quote is a very good description of what we can conclude from our research described in this section. Begin 2009, Rohm & Haas (in corporation with IBM Research GmbH) presented their results on this matter, using their LightLink™ material: "It was determined that the previous version of our clad, XP-5202A, was not suitable for use on flexible substrates. Cracking and delamination were observed for this clad during bending tests when it was coated on

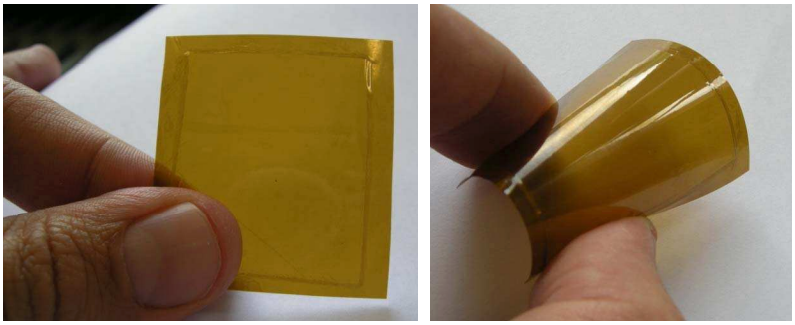

Figure 4.8: Laminated Truemode™ Backplane Polymer waveguide stack in between two Polyimide foils after lamination (left) and in bended state (right).

a flexible substrate. A research program was initiated to develop a flexible clad product that would be useful for building waveguides on flexible substrates. The resultant product, XP-07423A, is a modified version of the earlier clad product, XP-5202A, that was designed for rigid substrates, The XP-07423A can be used for both rigid and flexible substrates"[23]. In the same paper they present waveguides on top of a non-defined 190 μm thick flexible substrate, bended to a bending radius of 4 mm without deteriorating the waveguides. No such approach was found in literature concerning the Epocore / Epoclad , Ormocers® or Truemode™ Backplane Polymer material, but the same conclusions can be expected for these non-flexible materials.

The choice for Polyimide as foil is a very straightforward choice. Cheap material as PET (Polyethylene terephthalate) and PEN (Polyethylene Naphthalate) foils cannot be used due to their low glass transition (85 ^{o}Cand 125 ^{o}C respectively) with respect to the cure temperatures of the optical materials. For higher cost materials is Polyimide superior to other materials. Polyimide is the dominant material in the flexible circuits industry because of its numerous advantages including excellent flexibility at all temperatures, good electrical properties, excellent chemical resistance, very good tear resistance and a high glass transition temperature (up to 500^{o}C) [24].

4.5.1 Mounting

To be compatible with standard PCB process tools, the flexible foils must be attached to a temporary rigid carrier. For low temperature processing (e.g. silicones), this is often done with wax, but the high cure temperature of our polymers does not allow the use of wax. Doublesided tapes can hold the foil to some extent, but shrinkage and the higher CTE of the optical materials will

make the foil curl and pull off the tape when several layers are stacked. Tapes which hold high adhesion during high temperature processing, cannot be easily removed afterwards, resulting in damaging of the optical layers on top of the foil.

In the search for alternative mounting methods, a few were partly successful:

- Using the advantage of capillary effects, water or IPA can be deposited on the rigid substrate, followed by laying the foil on this fluid. The capillary effect will suck the Polyimide foil down during spinning, but during any baking step, the fluid will evaporate, releasing the foil. For Truemode™ Backplane Polymer , most of the curing happens during the room temperature UV exposure, which hardens the material as it is spincoated. All the other materials need prebake and will not be able to be hold in place using this method.

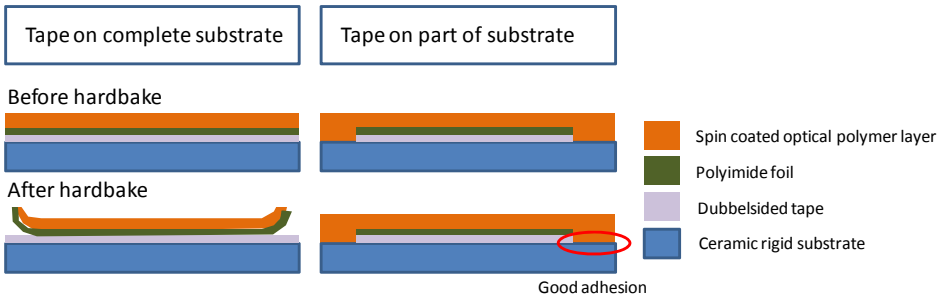

Figure 4.9: Edge adhesion approach for mounting of a Polyimide foil on top of a rigid substrate.

- Another alternative is the method of edge adhesion: The Polyimide foil is cut to a smaller size than the rigid substrate. At the edges, the optical material will be lying on top of the rigid substrate, and not on the Polyimide. This way the Polyimide foil is completely encapsulated and will not curl up. Figure 4.9 shows the schematic of this approach. This method is only viable for layers thicker than 50 μm . When spinning thinner layers, the material will not cover the edges of the Polyimide foil and again, the Polyimide will curl up. This means that LightLink™ and Truemode™ Backplane Polymer cannot be processed this way because of its spincoatable thickness limitation of about 35 μm .

4.5.2 Waveguide stack deposition

The adhesion of the optical polymers on the Polyimide foil is a crucial factor. It is decisive for the success of the layer deposition. Therefore we can split this

work in the different types of surface treatment for the Polyimide foil. This part of the research was executed in the first year of this PhD period, when Epocore / Epoclad and LightLink™ were not yet available. The results described in what follows are with Truemode™ Backplane Polymer , Ormocers® and SU-8. This latter is an epoxy based material, often used as master material because of its very good patterning properties like very high aspect ratios. The optical bulk loss of SU-8 is much higher than for the other materials (0.6 dB / cm).

Untreated Polyimide foil

All tested material show very brittle behavior after processing and peel off easily from the flexible substrate foil. Curling of the substrate after release is always observed, but is most significant for Truemode™ Backplane Polymer material. Figure 4.10 shows some examples.

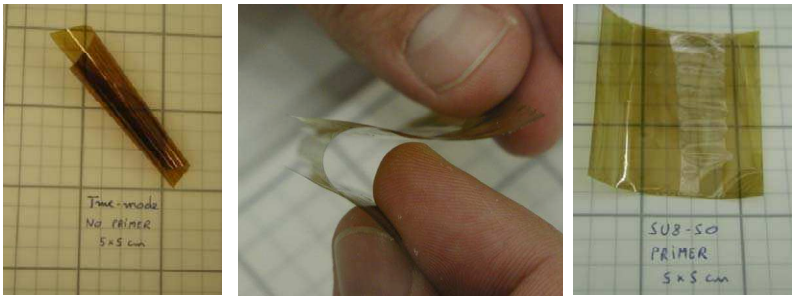

Figure 4.10: Examples of failure systems curling, cracking and delamination after processing of waveguide layers on top of an untreated Polyimide foil.

Primer coated Polyimide foil

Different primers for Polyimide are commercially available. These form a physical layer on top of the Polyimide and should enhance the adhesion with other layers on top of the Polyimide . Since there exist so many primers for each material, we limited ourselves to test the primers which were available in-house (VM652, TI prime). None of these primers resulted in a noticeable improvement, so no efforts were done to purchase other kind of primers.

Mechanical roughened Polyimide foil

Tests were performed with mechanically polished and with sandblasted Polyimide foil. The adhesion of the optical polymers was visible improved, but not

yet to an acceptable level. Figure 4.11 shows a microscopic picture of untreated and sandblasted Polyimide foil to show the modification of the surface.

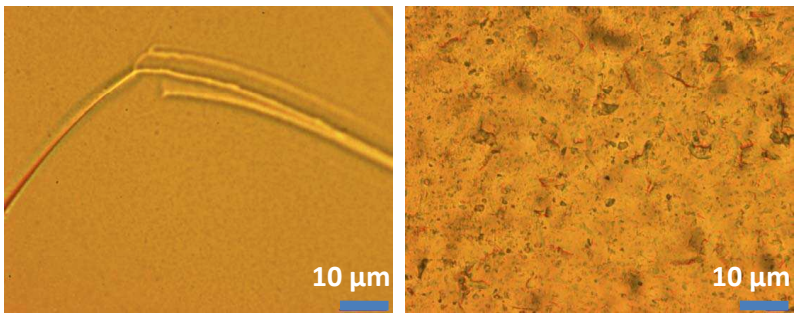

Figure 4.11: Microscopic picture of the surface of an untreated UPILEX S-25 Polyimide foil (left, the scratch is intentional to focus the microscope) and the same foil after sandblasting (right).

Oxygen plasma treated Polyimide foil

Oxygen plasma treatment is an expensive process step and difficult to implement in a production line, but is has proven to enhance the bonding energy between polymers and Polyimide significantly [4]. Two different oxygen plasma treatment recipies where put forward after showing their success in other research programs within CMST. The parameters for these recipies are shown in Table 4.2. The adhesion of all the polymers (SU-8, Truemode™ Backplane Polymer and Ormocers®) to the plasma treated Polyimide foil has significantly improved to an acceptable level, surviving the standard scotch tape testing.

Table 4.2: Oxygen plasma recipy parameters for the modification of Polyimide foil surfaces.

Menu	Gasflow 1 (scmm)	Gasflow 2 (scmm)	Power (W)	Pressure (mTorr)	Duration (min)	DC Bias Voltage (V)
1	CHF_3-5.0	O_2-20	150	100	5	337
2	CHF_3-1.2	O_2-23.7	100	150	5	-

4.5.3 Remarks, adjustments and results

- The CTE of the common flex Polyimide substrates for multilayer PCB's are typically low to match the low CTE of electronic active devices and SMD

components (Surface mount devices)[25]. This low CTE will always induce large CTE differences with existing waveguide materials and delamination and curling on foil are probably unavoidable. The CTE difference and shrinkage of the polymers clearly contributes to the curling of the substrate, because when the polymer layers are peeled off from the Polyimide foil, they do not curl anymore. A method to reduce the impact of the CTE difference is a slower ramping of the cure and cooling temperatures of the substrate. A clear relationship between temperature ramp and curling was seen, but the curling never disappears completely.

- The mounting of a Polyimide foil on a rigid carrier stays problematic as discussed in Section 4.5.1. Owing to this, the yield will be unacceptably low.
- When mounting was successful and the oxygen plasma treatment was performed, the final substrate can bend modestly. A minimum bending radius of 5 mm can be achieved, but the brittleness of the substrate is still too high which limits the handling dramatically. Figure 4.12 shows a bended SU-8 stack on a Polyimide foil (right) and the cross-section of a fracture of a Truemode™ Backplane Polymer stack on a Polyimide foil.

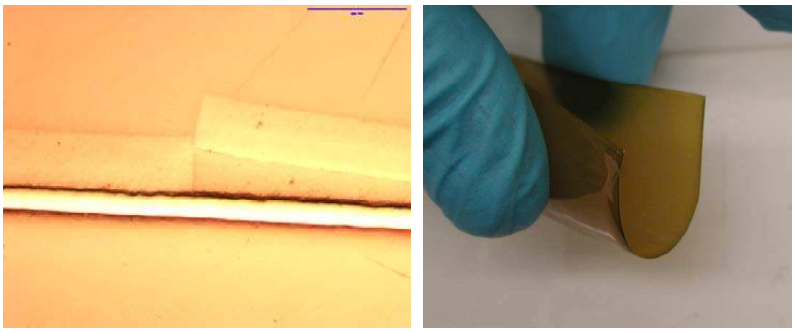

Figure 4.12: Cross-section of a fracture of a Truemode™ Backplane Polymer waveguide stack on top of a Polyimide foil (left) and a bended SU-8 layer stack on top of a Polyimide foil (right).

- During bending of the substrate in such a way that the outer side is the optical polymer side, these optical layers suffer from a high tensional stress. At places of disuniformity like waveguides, this stress will be even higher and the layer will be damaged locally. Pictures of this phenomena are shown in Figure 4.13.
- In the hope to release the tension inside a complete waveguide stack, efforts where done to combine Epocore / Epoclad , Ormocers® , Truemode™

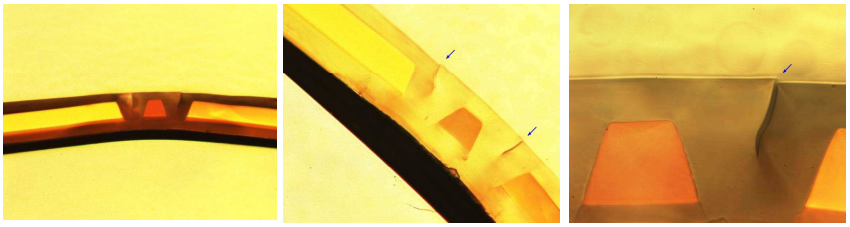

Figure 4.13: Damage of the optical layers at the waveguides due to a local peak in tensile stress in a Truemode™ Backplane Polymer waveguide stack on top of a Polyimide foil.

Backplane Polymer and SU-8 cladding and core layers (stacking of core and cladding layers from different materials). The work done to adjust the process flows and solve adhesion problems was quite extensive but will not be described in detail since no noticeable improvement was achieved.

4.5.4 Top Polyimide layer

A spin coated Polyimide layer on top of the stack improved the strength and brittleness of the total stack significantly, but inherently, flexibility was lost. The substrate seemed to be much stiffer due to the upper Polyimide layer.
Since the top Polyimide layer is only 8 μm thin and the bottom Polyimide foil 25 μm , there still exists a large asymmetry in the layer build-up, resulting in a different minimum bending radius in different directions. As can be expected, the substrate will fail easier at the thin Polyimide side as seen in Figure 4.14 where the top right photograph shows a breakage of the optical waveguide stack due to the breakage of the spin coated Polyimide layer. Another issue is the adhesion of the top Polyimide layer to the optical material, since bad adhesion results in a bad transfer of tensile strength and thus no actual physical support. This is clearly seen in the bottom pictures of Figure 4.14, where delamination occurs at the place of bending. The spincoating of the Polyimide layer and its compatibility with the different optical materials will be discussed in much more detail in next Section 4.6.

4.6 Waveguide stacking between spin-coated PI

A third approach consists of the sandwiching of the waveguide stack in between two spincoated Polyimide layer. Spincoated PI is a lot thinner than Polyimide foil + adhesive, so we can expect much higher flexibility than using lamination like described in section 4.4. The resulting stack is completely symmetrical, in comparison to the Polyimide foil / waveguidestack / spincoated Polyimide of

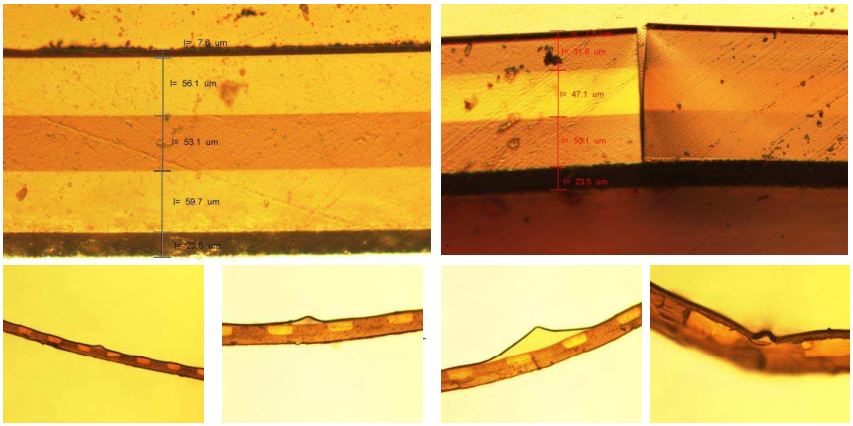

Figure 4.14: Truemode™ Backplane Polymer waveguide stack on top of a Polyimide foil and covered by a spincoated Polyimide layer (top left), breakage of the sample (top right) and delamination of the spincoated Polyimide layer (bottom).

Section 4.5.4 which is asymmetric and showed bad and asymmetric bending behavior.

This section describes a release method from the temporary rigid carrier and the compatibility of the spincoated Polyimide with the optical polymers and their process flow.

4.6.1 Flexible substrate release

As depicted before, the processing of all layers must be done on a temporary rigid carrier. This means we need a kind of approach to attach the spin coated layers to the carrier until the end of the processing and be able to release them afterwards. Hightec MC AG [26] uses a soluble release layer in between carrier and spincoated Polyimide for this matter, but keeps the information about the release layer material enclosed. Also laser induced release methods were reported in literature in recent years [27, 28, 29, 30, 31] but these techniques are not compatible with the infrastructure of CMST. Within the European project SHIFT (Smart High- Integration Flex Technologies [32]), the same need occurred for the release of flexible electronic circuits and UTCP's (Ultra thin Chip Package). The release method explained in this section was developed together with the people working on these projects.

The process step which did the trick was the selective use of an adhesion primer for Polyimide on a glass substrate. The method makes use of the very good

adhesion of Polyimide to glass using an adhesion promoter and the very poor adhesion when no primer is used. Therefore glass was chosen as substrate.
High quality white float glass was purchased from PGO [33], which has its main application as a substrate for optical coatings. The CTE of this material is 8.7 ppm/K which is typically for glass a very low CTE compared to that of the optical polymers (see Table 4.1 in Section 4.3). This is a very big disadvantage but the lack of any other existing and applicable release method forces us to make use of glass. The selectivity of Polyimide adhesion was also tested on silicon and FR4. Polyimide adheres quite well on FR4, which eliminates FR4 as substrate material for release. Silicon can also be used but is much more expensive and has an even lower CTE (2.6 ppm/K) than the white float glass. Figure 4.15 gives a schematic overview of the process flow of the used release method. The edges of the rigid glass carrier are covered with adhesion promoter (Pyralin^{TM} VM652 from HD Microsystems [14]) with a syringe. The primer is cured on a hotplate @ 120 ^{o}C for 60s. Then the bottom Polyimide , the optical waveguide stack and the top Polyimide layer are deposited and cured. At the end, the sample is cut out at the edges using a tripled frequency (355nm wavelength) Nd:YAG laser. The release of the sample after laser cutting can take a few minutes. Forcing the sample manually during release should be avoided.

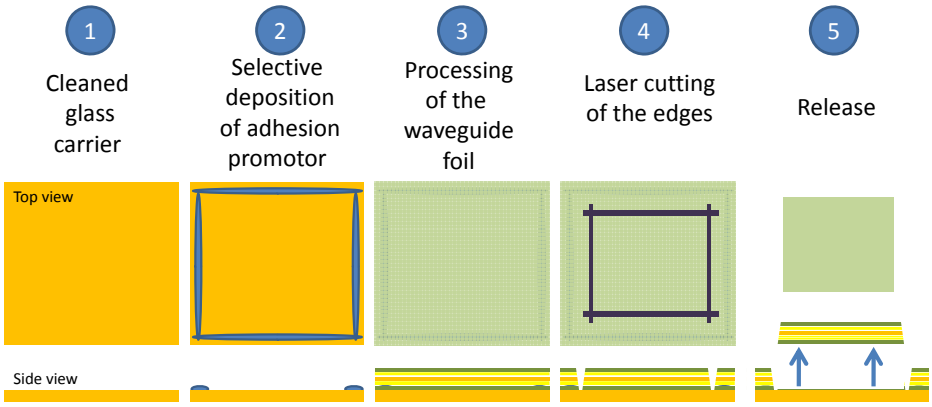

Figure 4.15: Schematic process flow of the release method for spincoated Polyimide on top of a float glass carrier, using selective adhesion promoter deposition.

The deposition of the adhesion promoter did not suffer from any problems in the beginning of this research, but at one point, the adhesion promoter started to contract on the glass surface. The reason for this is upto now not revealed. Possible change in glass or primer batch properties could have occurred without our knowledge. A solution to this problem is the mechanical roughening of the glass edge surface to higher the surface energy locally. Other solutions have been

proposed by cleaning the glass substrates thoroughly in an RBS based solutions following the procedure in Table 4.3.

Table 4.3: Cleaning procedure for white float glass substrate to overcome the contraction problems with the adhesion promoter.

Process step	Process parameters
Manually cleaning with wipes	Acetone
	IPA
Cleaning bath	5%RBS/95%water solution ; 12 hours
Ultrasonic agitation	5%RBS/95%water solution ; 5 minutes
Rinse	DI water
Ultrasonic agitation	DI water ; 5 minutes
Rinse	IPA
Rinse	water
Dry	N_2 pistol

Concerning the long duration and work intensity it is obvious that this latter method is only profitable when large amounts of substrates are needed. For laboratory use, the edge surface roughening is a much cheaper and faster process.

4.6.2 Compatibility of undercladding layer with bottom Polyimide layer

Polyimide material choice

Together with the provider of spincoatable Polyimide , HD Microsystems [14], the choice of Polyimide material was made driven by CTE and cure temperatures. CTE differences define the risk of delamination of the stacked layers, while the adhesion strength of the Polyimide-polymer interface defines the strength and flexibility of the final stack. Therefore the PI2525 type Polyimide with a CTE of 40 ppm/K was chosen. This material also has a significant lower imidization- (or cure-) temperature than most other Polyimide materials (210 ^{o}C versus typically 350 ^{o}C). This is important regarding the degradation temperatures of the investigated optical materials, which are often lower or equal to 350 ^{o}C. Table 4.4 gives an overview of the thermal stability of these polymers.

The main properties of the PI2525 type spincoatable Polyimide are summed up in Table 4.5.

Spincoated Polyimide layers are limited in thickness ($\leq$ 10 μm). When higher thicknesses need to be obtained, fully cured Polyimide layers can be stacked on top of each other if they are oxygen plasma treated. The process flow to obtain a $\pm$ 10 μm thick PI2525 layer is given in Table 4.6. Most Polyimide materials shelf

Table 4.4: Thermal stability of the investigated optical polymers.

Optical waveguide polymer	Degradation temperature
Truemode™ Backplane Polymer	350 ^{o}C
Ormocers®	280 ^{o}C
Epocore / Epoclad	230 ^{o}C
LightLink™	350 ^{o}C

Table 4.5: Main properties of Polyimide PI2525 from HD Microsystems.

Tensile Strength	13.1	kg/mm^2
Elongation	10	%
Modulus	245	kg/mm^2
Stress	3.6 x 10^8	dynes/cm^2
Moisture uptake	2-3	%
Dielectric constant	3.3	@ 1 kHz, 50 % RH
CTE	40	ppm/K
Glass Transition Temperature	320	^{o}C
Decomposition Temperature	560	^{o}C
Refractive index	1.70	-
Viscosity in solution	60 $\pm$ 10.0	Poise

life can be drastically improved by freezing the Polyimide when not used. This means we have to defrost the material 1 hour before we want to start processing. The deposition of PI2525 can be done with a large pipette. Air bubble insertion must be avoided during deposition, but Polyimide is not very sensitive to this. If air bubbles are inserted, they are clearly visible and be removed using a pipette before spinning. Because of the high viscosity of the fluid Polyimide, there is no need for manual tilting of the substrate to assure complete coverage of the sample as that is the case for Truemode™ Backplane Polymer and LightLink™ . The spinning process itself is done in two steps, first the material is spread over the substrate at a lower spin speed and in a next step brought to the right layer thickness at a high spin speed. This is to optimize the layer thickness uniformity and prevent the occurrence of uncovered sample areas.

Truemode™ Backplane Polymer

Truemode™ Backplane Polymer cladding material can be spincoated on top of a PI2525 without any problem. Truemode™ Backplane Polymer adheres very good to PI2525 after curing. When breaking a stack of Polyimide 2525 with a Truemode™ Backplane Polymer cladding layer, the break line is exactly the same for both materials, meaning that even under the highest possible stress, the layers

Table 4.6: Process flow for a $\pm$ 10 μm thick PI2525 layer.

Process step	Process parameters
spincoat	10s @ 500 rpm and 50s @ 2000 rpm
hardbake (imidization)	In N_2 vacuum oven
	Temperature ramping from 20 to 210 ^{o}C @ 4 ^{o}C/min.
	Temperature dwell @ 210 ^{o}C for 180 min.
	Temperature ramping from 210 to 20 ^{o}C @ 2 ^{o}C/min.

will not delaminate from each other.

Epocore / Epoclad

Same conclusions can be drawn for Epocore / Epoclad cladding material as for Truemode™ Backplane Polymer cladding.

LightLink™

The LightLink™ cladding material can be spincoated on top of a PI2525 without any problem. However, after curing, the LightLink™ cladding layer shows poor adhesion to the PI2525 layer. Oxygen plasma treatment of the Polyimide layer did not result in any improvement. Since Truemode™ Backplane Polymer cladding adheres very well to the PI2525, it was tried as adhesion material between the PI2525 and the LightLink™ cladding with success. LightLink™ cladding can be spincoated on top of a cured Truemode™ Backplane Polymer cladding material without any problem with good adhesion after curing.

Ormocers®

The Ormocers® cladding material contracts in a hydrofobic way on top of a PI2525 layer after spinning. Plasma treatment of the PI2525 layer did not resolve this issue. Using Truemode™ Backplane Polymer as an adhesion layer in the same way as done with LightLink™ was tested, but Ormocers® contracts in the same way on Truemode™ Backplane Polymer cladding as it does on PI2525. The use of PI2611 from the same provider HD Microsystems[14] instead of PI2525 was tried out. After plasma treatment of the PI2611 layer, the Ormocers® cladding layer can be spincoated without any further problem with modest adhesion after curing. The PI2611 is a more typical PI with lower CTE ($\leq$10 ppm/K) and higher imidization temperature than PI2525 ($\geq$ 300 ^{o}C). This means that the curing of the top PI2611 layer will damage the optical material underneath due to the high temperature. When curing the top PI2611 at 210 ^{o}C it will imidize only

partly. This results in a inferior top Polyimide layer, but with respect to the flexibility testing and the optical bending loss measurements for Ormocers®, it is still advisable to work on with this Polyimide type.

4.6.3 Compatibility of top Polyimide layer with uppercladding layer

Truemode™ Backplane Polymer

PI2525 can be spincoated on top of a Truemode™ Backplane Polymer cladding without any problem. PI2525 adheres very well to Truemode™ Backplane Polymer cladding after curing. When breaking a stack of Truemode™ Backplane Polymer cladding with a PI2525 layer, the break line is exactly the same for both materials, meaning that even under highest possible stress, the layers will not delaminate from each other.

Epocore / Epoclad

Same conclusions can be drawn for Epocore / Epoclad cladding material as for Truemode™ Backplane Polymer cladding.

LightLink™

PI2525 can be spincoated on top of a LightLink™ cladding layer without any problem. However, after curing, the PI2525 cladding layer shows poor adhesion to the LightLink™ cladding layer. Oxygen plasma treatment of the LightLink™ layer did not result in any improvement. Again, Truemode™ Backplane Polymer cladding was tried as adhesion material between the PI2525 and the LightLink™ cladding, but Truemode™ Backplane Polymer cladding contracts on top of a cured LightLink™ cladding layer after spinning. Plasma treatment of the LightLink™ cladding layer resolved this problem. The complete stack of bottom PI2525, LightLink™ waveguide stack and top PI2525 layer with intermediate Truemode™ Backplane Polymer cladding adhesion layers shows very good adhesion. When breaking such a stack, the break line is exactly the same for all materials, meaning that even under highest possible stress, the layers will not delaminate from each other.

Ormocers®

PI2525 cannot be spincoated on top of an Ormocers® layer, even when it is plasma treated, the PI2525 material will still contract after spinning. PI2611 can be spincoated on top of an Ormocers® layer without any problem. Adhesion

however after curing is poor. PI2611 has an imidization temperature of about 350 ^{o}C, which means that curing at 210 ^{o}C will result in a inferior uncured layer, but we will accept this temporarily to characterize the Ormocers® material during bending.

4.6.4 Total hardbake

The curing temperatures of the optical polymer is 150 ^{o}C while the curing temperature of the top Polyimide layer is 210 ^{o}C. To avoid any more outgassing of the optical polymer during this latter heating cycle, the stack is cured at 215 ^{o}C during 1 hour before the spincoating of the top Polyimide layer.
When bringing a complete waveguide stack of Epocore / Epoclad material at such high temperatures, the layers will crack during the cool down process, due to the high CTE difference between Epocore / Epoclad and the glass carrier. This problem does not occur with Ormocers® , Truemode™ Backplane Polymer or LightLink™ , contradictory to their even higher CTE difference with respect to the glass carrier. This is explained by the lower Y-modulus for these materials, which means that they can take up more stress before breaking than the Epocore / Epoclad . By lowering the cooling rate and thus the temperature ramp, the appearance of cracks can be reduced, but not completely avoided. The solution for this is the early release of the stack from its glass carrier before this 210 ^{o}C temperature step. The Epocore / Epoclad waveguide stack is quite stiff and spincoating of the top Polyimide layer can be done without the mounting of the stack onto another rigid carrier. No curling of the substrate occurs during the curing of this top Polyimide layer due to the small thickness of this layer ($\leq$ 10 μm) and the stiffness of the Epocore / Epoclad stack.

4.6.5 Flexible waveguide foil

Figure 4.16 shows images of the side, front and bottom view of a Truemode™ Backplane Polymer flexible finished waveguide foil and pictures of the waveguide foil during bending. Figure 4.18 in Section 4.7 shows cross-sections of waveguide foils fabricated in LightLink™ and Epocore / Epoclad material.

4.7 Characterization of the flexible waveguide foils

4.7.1 Optical propagation losses

The optical propagation loss of optical waveguides can be unraveled in following terms:

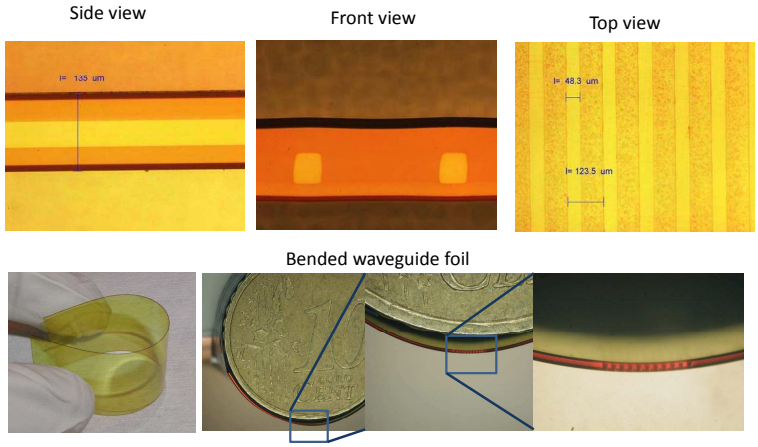

Figure 4.16: Side, front and top view of a Truemode™ Backplane Polymer flexible WG-foil using spincoated Polyimide (top) and bended state pictures.

$L_{waveguide}$ = $L_{absorption}$ + $L_{scattering}$ + $L_{extrinsic}$
$L_{absorption}$: In polymers, optical losses comes from two main sources: electronic absorption and vibrational absorption. For a wavelength of 850 nm, the most significant contribution comes from the vibrational absorption.
$L_{scattering}$: For a homogeneous material without any structure on the scale of a wavelength of light, the dominant scattering that occurs is Rayleigh scattering.
$L_{extrinsic}$: All optical loss caused by larger scale phenomena as voids, cracks and surface roughness.

None of the fabricated waveguides shows visual voids or cracks but the surface roughness will always be present. The roughness of photolithography waveguides is investigated in detail in Section 3.3.3 in Chapter 3, concluding that the Epocore / Epoclad suffers from the highest surface roughness and that LightLink™ has the smoothest surface. Truemode™ Backplane Polymer is somewhere in between. The Ormocers® shows relative low roughness but poor waveguide cross-sectional profile control.

The absorption and scattering loss are difficult to assess or to define in an easy experiment. The cure temperature of the top Polyimide layer of 210°C is applied for 3 hours. This temperature is well above the glass temperatures of the investigated optical polymers. It is hard to tell if this process step has a significant impact on the scatter and/or absorption losses. A detailed study on the unraveling of the optical propagation losses in its components is complex and time-consuming and out of the scope of this work. Therefore this section is lim-

ited to the quantification of the total optical propagation loss.

Traditional optical waveguide propagation loss measurement methods include waveguide direct cut-back [34], prism coupling [35], scattered light collection [36, 37], FabryPerot cavity measurement [38, 39] and multiple reflections detection [40, 41]. All of these methods have inherently uncertain factors which can affect measurement precision, so every measurement result must be analyzed with care and sense for measurement value corrections. Some methods have higher demands than other for the waveguide that needs to be measured. Some can only be applied on buried waveguides or waveguides with a large length. At CMST, a Newport [42] optical measurement set-up is available which allows us to do cut-back measurements. The only demand for cut-back measurements is the need to cut the waveguides. This is a simple process for rigid waveguides on FR4, but on flex substrates this gets trickier, as will be explained later on in this section.
In cut-back measurements, the propagation loss is calculated by comparing two optical powers before and after waveguide cutting, obviously, this method has two uncertain factors: first, the facet of the waveguide before and after cutting cannot keep the same condition and secondly, fiber coupling efficiency before and after cutting cannot be kept constant either. We can however try to keep the waveguide facet and coupling efficiency within a certain small window, so that the uncertainties are limited.

Measurement set-up

Measuring the optical propagation losses of a waveguide consists of sending light with the right wavelength into one end of the waveguide and measure the power of the light coming out at the other end of the waveguide. The difference in optical power between in-coupled and out-coupled light is then a quantification of the optical losses of the waveguide.

Figure 4.17 shows the main building blocks of the used optical measurement table. The used light is produced by a laser diode light source from QPhotonics [43] operating at 845nm and is mounted in a Newport [42] laser diode mount (Model 742 DIL Mount), allowing the interface to a Newport (Model300B Series) temperature controller, and a Newport (Model 500B Series) laser diode driver. Measurements are performed using a laser operating current of 32mA. To couple this light into the waveguide, an optical step index fiber with core diameter of 50 μm and NA (numerical aperture) of 0.2 is coupled with the laser diode at one end, and mounted on a motorized XYZ stage on the other end. This optical fiber is about 20 m long to perform mode scrambling. The stage will bring the fiber in alignment with the waveguides of the sample, which is mounted on the sample stage. The X,Y and Z-movements can be done manually by micro-screws,

automatically with the motion controller device or can even be programmed and driven with software on the PC next to the set-up. Since this software was not completely functional at the time of these measurements, it was not used. This does not affect the resolution of the measurement but increases the measurement time. The outgoing light of the sample waveguides is guided to a Newport photodetector (818 Series) with another optical fiber. This fiber has a core diameter of 62.5 μm , an NA of 0.275 and is mounted at one end on an XYZ stage and coupled to the photodetector at the other end.

Fast alignment was done by operating the XYZ stages manually. Two CCD cameras ease this process by allowing us to visually follow the movements of the optical fibers with respect to the optical waveguide facets. One camera focuses on the in-coupling facet and one on the outgoing facet. The in-coupling optical fiber is aligned with the in-coupling facet of the waveguide until we see a very clear light spot coming out of the waveguide out-coupling facet. The camera at the in-coupling side allows us to control the distance of the optical in-coupling fiber to the waveguide facet with an estimated accuracy of 10 μm . The fast alignment of the out-coupling fiber is done visually using the out-coupling camera, again with an estimated accuracy of 10 μm .

Precise alignment is done actively using the optical power meter. The movement of the 2 XYZ stages is done with the motion controller to have a motion accuracy of about 1 μm . Moving the in- and out-coupling fibers allows us to define the point of maximum light transition when the highest value on the optical power meter is reached. We can say the maximum possible alignment is achieved.

The optical path from laser diode to photodiode has multiple sources of optical loss. Most of these losses can be eliminated in the final results by making a reference measurement. This measurement consists of the alignment of the in-coupling and out-coupling fiber against each other in absence of the waveguide sample. The measured optical power by the photodiode is then the reference optical power. The eliminated optical losses using this technique are:

- Coupling loss from the laser diode to the optical in-coupling fiber
- Coupling loss from the optical out-coupling fiber to the photodiode
- Propagation loss inside the in- and out-coupling optical fiber
- Losses due to numerical aperture difference of in-coupling and out-coupling fiber

By doing these reference measurements every time we use the optical measurement set-up, we assure that irregularities in the set-up are detected early in the measurement, since the set-up is used by different people and for different purposes.

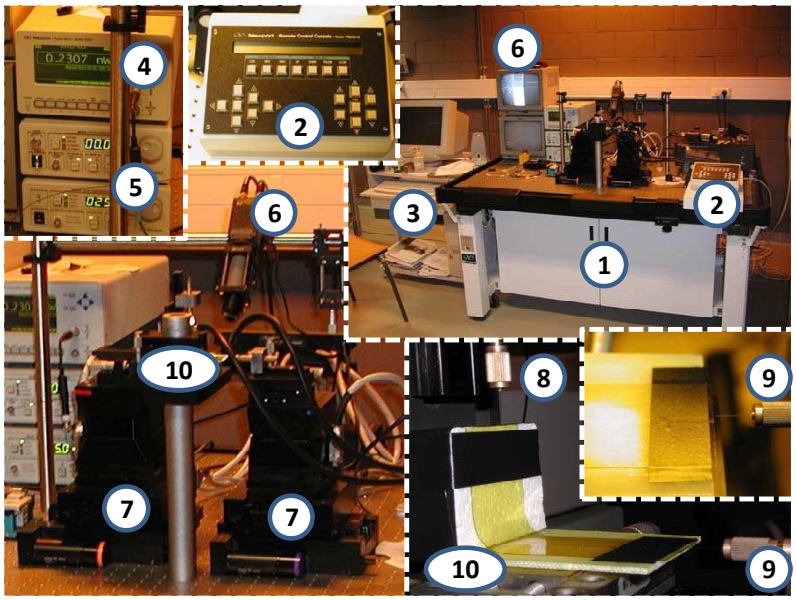

Figure 4.17: Newport optical measurement bench set-up for waveguide optical loss measurements.

Waveguide facet preparation

The roughness of the end facet of the waveguides is very important since it has a large impact on the coupling efficiency between the optical fiber and the waveguide. When doing cut-back measurements, the difference in total optical waveguide loss is monitored for different lengths of the waveguide. Comparing these values will eliminate the loss caused by the facet roughness since it is the linear factor that defines the propagation loss. This is however only the case when the facet roughness is identical for each measurement. Because the same waveguide has to be cut all over again after each measurement, the facet roughness will be different every time. In other words: the higher the roughness of

the waveguide facet, the higher the variation on the optical losses caused by the waveguide facet, the lower the accuracy of the propagation loss measurement. Rigid waveguides on FR4 boards can be easily sawed and polished at both sides to an end roughness well below the 850 nm optical wavelength of the used light, reducing the impact of the facet roughness to a minimum. Flexible waveguide on the contrary cannot be polished easily to such a low roughness, since the flexible behavior of the substrate is a problem in the mechanical polishing procedure. Alternative waveguide termination techniques must be explored to keep the waveguide facet roughness within an acceptable value. Laser ablation has proven its success many times for the creation of optical facets like mirrors [44], lenses [45] and waveguides [46], so this technique looks like the obvious choice considering that laser ablation will be frequently used in the rest of this work for the creation of cavities, micro-mirrors, micro-via's, etc.

Figure 4.18 shows a picture matrix of waveguide facets fabricated with different techniques and different parameters for Truemode™ Backplane Polymer , LightLink™ and Ormocers® materials. For each facet, a back lighting and front lighting image was taken to show the surface texture and the waveguide locations.
Laser ablation of an Epocore / Epoclad flexible waveguide foil resulted in facet (a). The facet looks very bad and further trials pointed out that the flexible waveguide foil carrier during laser ablation (a ceramic substrate) was the cause of this. Clamping the waveguide foil in between two ceramics, so that the facet is sticking out in the air instead of lying on top of ceramic material was the solution. The laser ablated facet looks then like facet (b) with still a lot of deep grooves visible. The optimum laser ablation parameters are:

- Laser: Excimer laser 248 nm
- Projection mask: 1000 x 3000 μm ^{2}
- Laser regulate power: 12 mJ
- Attenuation: 0
- Fluence: 252 mJ/cm^2
- Translation speed: 120 μm /s
- Repetitions: 1x

Further investigations revealed that the grooves are mainly a result of the irregular Polyimide layer ablation. The edge of the ablated Polyimide layer is very coarse, which inflicts with the ablation of the underlying layer. A solution for this is an additional selective Polyimide ablation step, which removes the Polyimide layer locally above the future facet, without ablating the Epocore / Epoclad

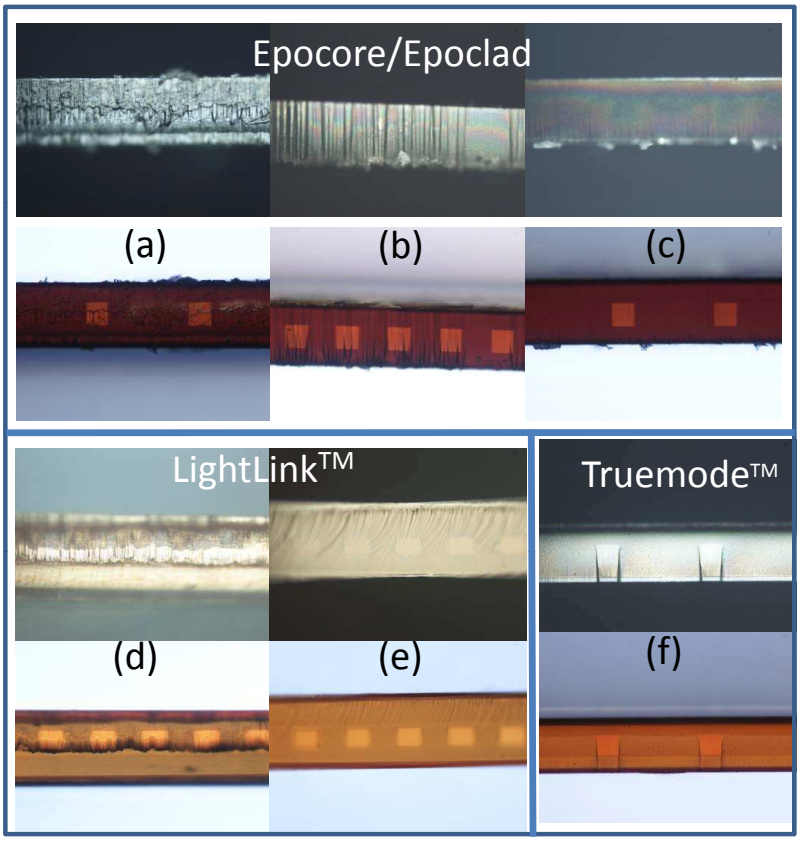

Figure 4.18: Picture matrix of flexible waveguide facets fabricated with different techniques and different parameters for Truemode™ Backplane Polymer , LightLink™ and Ormocers® materials

material. In a next step, the Epocore / Epoclad layers are ablated, which do not longer suffer from the Polyimide coarse layer edge. Facet (c) is the result. Small grooves are still visible in the uppercladding layer of the flexible waveguide foil, but not on the waveguide facets. The laser ablation parameters for the removal of the Polyimide layer are the same as shown above for the Epocore / Epoclad material, but with a much higher translation speed of 10000 μm /s. This way a strip of 100 μm width of Polyimide is removed. Removing two strips next to each other is enough to create a Polyimide free area.
Same principles were applied for the LightLink™ waveguide foil, but this material shows bad ablation behavior in all parameter operating windows. Facet (d) shows the irregularities on the LightLink™ surface after ablation. A good alter-

native is the breakage of the flexible waveguide foil by bending it to an extensive bending radius of 1 mm. The fracture (Facet (e)) of the waveguides looks very smooth, only surface damage is witnessed in the cladding layers. This method is easy but has a lot of limitations like the unknown exact location of the fracture. For the cut-back measurements however it will do.
Truemode™ Backplane Polymer material has a very good laser ablation behavior and results in smooth surfaces. Facet (f) is the result using the same ablation parameters as those depicted above for Epocore / Epoclad waveguide foils.

Cut-back measurement results

The results of the cut-back measurements are shown in Figure 4.19. The Epocore / Epoclad sample broke by handling during the measurement process, which restricted the amount of measurement points to 2, reducing the reliability of the propagation loss value of 0.89 dB/cm. The LightLink™ flexible waveguides shows the lowest losses of 0.27 dB/cm. For the Ormocers® material, we noted before that is is very hard to fabricate waveguides due to the proximity UV exposure mode. In Section 3.3.3 of Chapter 3, we explained the substrate tilt problem when the waveguide substrate is not perfectly parallel with the projection mask. For cut-back measurements, we need waveguides which are as long as possible, but the larger the substrate the more significant this tilt problem can become. The 8 cm long Ormocers® waveguides fabricated for the cut-back measurements appeared to touch each other due to the large distance during the UV proximity exposure between the mask and substrate. Consequently, all the light emitted in 1 waveguide will be spread over all the waveguide of the sample, which makes the waveguides un-useful. No other attempts were done since the reproducibility of the fabrication process is too low.

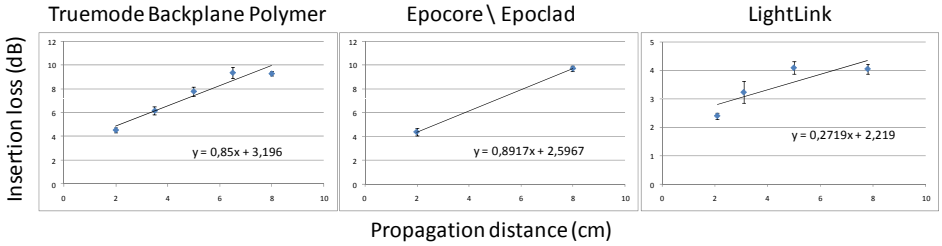

Figure 4.19: Cut-back optical waveguide propagation loss measurements for Truemode™ Backplane Polymer , Epocore / Epoclad and LightLink™ flexible waveguides.

The resulting optical propagation loss of Truemode™ Backplane Polymer dry film flexible waveguides is 0.85 dB/cm. This is a much higher value than expected. The providers claim that Truemode™ Backplane Polymer waveguide

show losses of 0.05 dB/cm [15] and a study on laser ablated waveguides in wet film core Truemode™ Backplane Polymer showed a loss of 0.13dB/cm [46] on FR4 boards (see Figure 4.20). The main differences between these latter rigid waveguides and the flexible waveguides presented in this work are the fabrication technique (laser ablation versus photolithography respectively), the cure temperature (150^{o}C for 1 hour versus 210^{o}C for 3 hours respectively), the material (wet film versus dry film Truemode™ Backplane Polymer) and the waveguide facet (polished versus laser ablated).

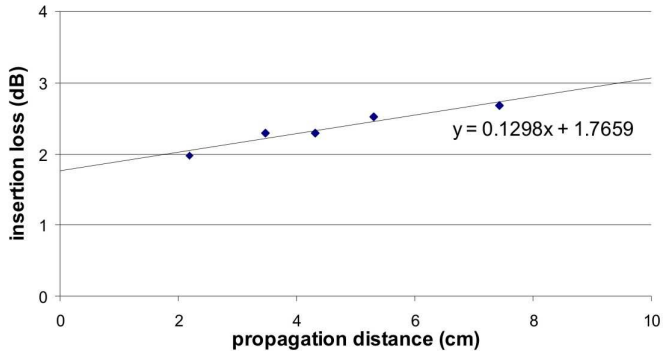

Figure 4.20: Cut-back optical waveguide propagation loss measurement for wet film Truemode™ Backplane Polymer laser ablated waveguides (Source: PhD-thesis Geert Van Steenberge)

The influence of the waveguide facet should be limited due to the averaging affect over the different measuring points. The difference in optical losses between dry and wet film formulation Truemode™ Backplane Polymer should also be very small according to the literature and material data sheets. This leaves the cure temperature and fabrication technique. In an attempt to see the influence of the cure temperature, 2 identical rigid waveguides samples were fabricated on FR4 board and cured at 150^{o}C for 1 hour and 210^{o}C for 3 hours. A comparison of the total optical loss of the waveguides is shown in Figure4.21.

The difference is astonishing. The waveguides cured at 210^{o}C show 2.75 dB/cm more optical propagation loss than those cured on 150 ^{o}C. If the high temperature was the only cause of this waveguide deterioration, we should see the same loss for the flexible waveguides which is not the case. Possible reason is the effect of the FR4 substrate on the waveguides. At 210 ^{o}C the FR4 boards color changes from yellowish to brown. Some chemical changes took place inside the FR4 substrate, which indicates that some outgassing could occur from the FR4 substrate inside the highly expanded optical polymers on top of the FR4 board. We cannot draw conclusions about what effect has the highest contribution to the quite high propagation losses of Truemode™ Backplane Polymer dry film flexible waveg-

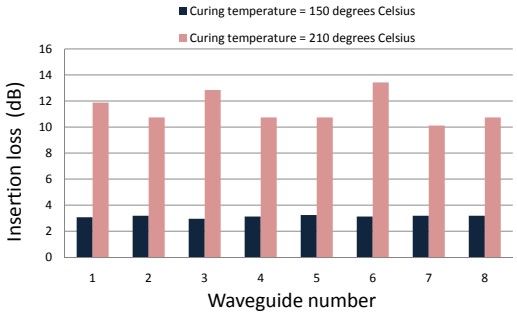

Figure 4.21: Optical insertion loss measurements for 3 cm long Truemode™ Backplane Polymer rigid optical waveguides on an FR4 board, cured at 150^{o}Cand at 210^{o}C.

uides. As said in the introduction of this subsection, it is out of the goal of this PhD thesis to determine these contributions.

4.7.2 Mechanical bending tests

Set-up

Standard bending tests and requirements for optical communication on flexible substrates does not exist at this moment. In this study a lot of possibilities were considered to build a set-up to quantify the bendability of flexible waveguides. Many set-ups used in literature use cylinders for the bending and weights on the sample to make it follow the curve of the cylinders. These weights however induce a tensile strength inside the sample, which is not favorable. Tensile force resistance and bendability should be clearly separated. Only few set-ups can perform bending without stretching the waveguides. The automation of these set-ups however is very complex and costly.

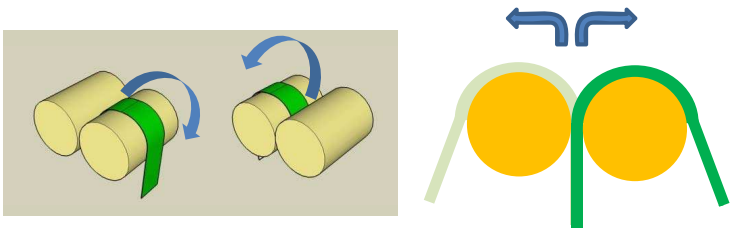

Figure 4.22: Bending test set-up for flexible optical waveguide foils

The manually bending process used to qualify (not quantify!) the flexibility of the

waveguide foils is shown in Figure 4.22. One end of the foil is clamped between two identical cylinders and the foil is than manually bended over the left and right cylinder consecutively; 1000 bending cycles take about 45 minutes. Quite time consuming but still a much faster and cheaper approach than the automatic version.

Bending tests results

Optical waveguide foils in the four investigated optical materials with a length of 8 cm and a width of 2 cm were tested on the set-up described above. Bending over three different bending radii was tested by using cylinders with a different radius (12.5, 4.5 and 2.5 mm). The waveguide foils were bended for three times to check the feasibility of the bending over the different bending radii and consecutively for 1000 times to evaluate the bending endurance. This difference was made because of the variety in applications, were bending cycles can vary from 1 in static non-flat surface applications to more than 1000 in dynamic hinge-like applications.

Table 4.7 shows the results. The notation "ok" means that the foil showed no visible defects and was considered intact. The notation "sample broken" means that the waveguide foil was broken along its transversal axis (2 cm wide axis) in two pieces due to the undergone bending cycles. To determine possible invisible damage to the waveguides, the optical propagation losses of the waveguides in flat status were measured before and after the bending test and compared with each other. The measurement resolution is about 0.5 dB. Losses below this value are assumed to be negligible and are referred to in Table 4.7 as zero. For a bending radius of 2.5 mm, we see for the Truemode™ Backplane Polymer material waveguide foil an additional loss of about 1 dB. It is difficult to determine if this small and acceptable optical devaluation is caused by micro-defects or by permanent changes of the material chemical bonds induced by the rather extreme bending conditions. The additional optical losses of about 3 dB for the Epocore / Epoclad waveguides at a bending radius of 4.5 mm is more significant but still acceptable considering the large amount of bending cycles.

4.7.3 Optical bending losses

The optical bending loss of a waveguide is the additional loss incorporated with the bending of waveguide. When the waveguide is brought back in a flat unbended status, this bending loss is zero. Bending loss occurs due to the change in angle of the cladding-core interface with respect to the propagating light. The conditions needed for total internal reflection inside the waveguide can so be violated for a certain fragment of the propagating light, which will be consequently be coupled out the waveguide resulting in an additional optical loss.

Table 4.7: Bending tests results for optical waveguide foils in Truemode™ Backplane Polymer , Epocore / Epoclad , LightLink™ and Ormocers® material .

Visual evaluation of the WG-foil after 3 times bending				
Bending radius (mm)	Truemode™ Backplane Polymer™	Epocore/ Epoclad	LightLink™	Ormocers®
12.5	ok	ok	ok	ok
4.5	ok	ok	ok	sample broken
2.5	ok	sample broken	sample broken	sample broken

Visual evaluation of the WG-foil after 1000 times bending				
Bending radius (mm)	Truemode™ Backplane Polymer™	Epocore/ Epoclad	LightLink™	Ormocers®
12.5	ok	ok	ok	ok
4.5	ok	ok	sample broken	sample broken
2.5	ok	sample broken	sample broken	sample broken

Additional optical insertion loss for an 8 cm long flexible waveguide after 1000 times bending (dB)				
Bending radius (mm)	Truemode™ Backplane Polymer™	Epocore/ Epoclad	LightLink™	
12.5	0	0	0	
4.5	0	2.83 $\pm$0.39	na	
2.5	1.08 $\pm$0.42	na	na	

Measuring the bending loss is done with the different set-ups shown in Figure 4.23, using cylinders with a radius of 12.5, 4.5 and 2.5 mm. The 8 cm long (2 cm width) waveguide foils are bended multiple times around the cylinders as depicted in Figure 4.23. The optical bending loss is then the difference between the measured optical propagation loss in bended and in non-bended state. The used set-up and the optical launch conditions are the same as described in detail for the propagation losses of unbent optical waveguides in Section 4.7.1. Figure 4.24 shows the results. The total bending loss for each set-up is shown in the left graph and the recalculated losses per centimeter of bended waveguide length is displayed in the right graph. The higher bending losses for Epocore / Epoclad is expected since the material has the lowest optical numerical aperture. When a material has a higher numerical aperture, the acceptance angle of a light ray incidenting the core-cladding interface will be higher. This means that more light

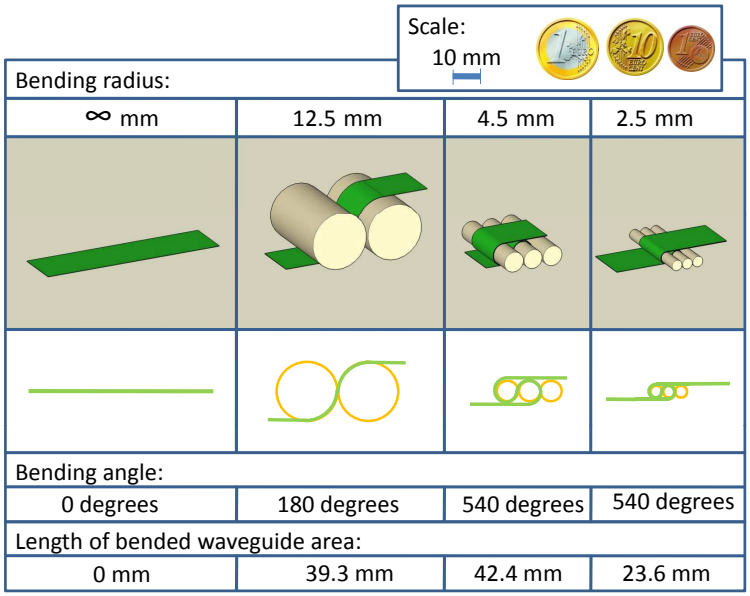

Figure 4.23: Optical bending loss measurement set-up for bending radii 12.5, 4.5 and 2.5 mm.

will fulfill the requirements for total internal reflection and thus more light will be guided through the bent area. The numerical aperture of Truemode™ Backplane Polymer , LightLink™ and Epocore / Epoclad are 0.34 ; 0.26 ; 0.18 repectively. These values are dependant on the refractive index difference between the cladding- and the core material. The providers of all these material are able to tune the refractive indices, and thus the numerical aperture of their material.

Since the flexible waveguide market is still limited nowadays, no standard requirements are put forward concerning the bending losses. The length of bended waveguide and the bending radius is purely dependent on the aimed applications. Therefore, rather than saying that the optical bending losses are acceptable, we compare them to the reported bending losses in the world's state-of-the-art. Figure 4.25 shows the bending losses of our Truemode™ Backplane Polymer , LightLink™ and Epocore / Epoclad flexible waveguide foils in a bending loss per cm versus bending radius graph. In the same graph, all the bending losses reported on flexible waveguides (as to our knowledge) are included referred with an "X". In some publications, the bending losses are given for different bending radii, in others only for one bending radius. The X's with the same color belong to the same publication. The included papers are listed here: [1],[47],[3],[48],[49],[50],[51],[52],[5],[53],[8],[54],[9],[55]. More details about these

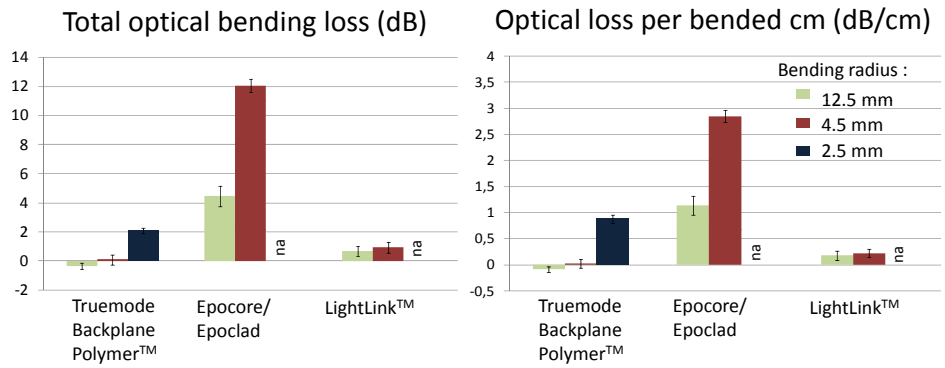

Figure 4.24: Total optical bending loss (left) according to the set-ups in Figure 4.23 and the recalculated losses per centimeter of bended waveguide length (right) for Truemode™ Backplane Polymer , Epocore / Epoclad and LightLink™ flexible waveguide foils.

publications are also included in Figure 2.5 in Section 2.3.5 in Chapter 2. The comparison of our flexible waveguides with these of the literature shows us that the state-of-the-art waveguides are more flexible when looking at the minimum bending radius of 1 and 2 mm. This issue is extensively discussed in Chapter 2. We see however that the optical bending losses of LightLink™ and Truemode™ Backplane Polymer waveguide foils are comparable to the ones reported by other research groups. The Epocore / Epoclad waveguide foils show much higher losses.

4.7.4 Conclusions

Different approaches for the realization of physically bendable waveguides were presented, all based on the use of a Polyimide foil or layer to support the non-flexible waveguide layer stack which was presented in Chapter 3. Application of this method in literature was briefly discussed, followed by the realization of such a foil inside this PhD work. A first approach consists of the lamination of a waveguide layer stack in between two Polyimide foils. Therefore the fabricated waveguide layers must be released from its temporary rigid processing carrier. Many different techniques were investigated, with only one peel-off technique and one sacrificial layer method showing satisfactional results.

The released waveguide stack laminated between two 25 μm thick Polyimide foil can be bended but the minimum bending radius of 10 mm is rather large. In a second approach, the waveguides were fabricated directly on top of a Polyimide foil. Many efforts were done to optimize the adhesion of the waveguide material with the inert Polyimide foil. Plasma etching showed to be the only method

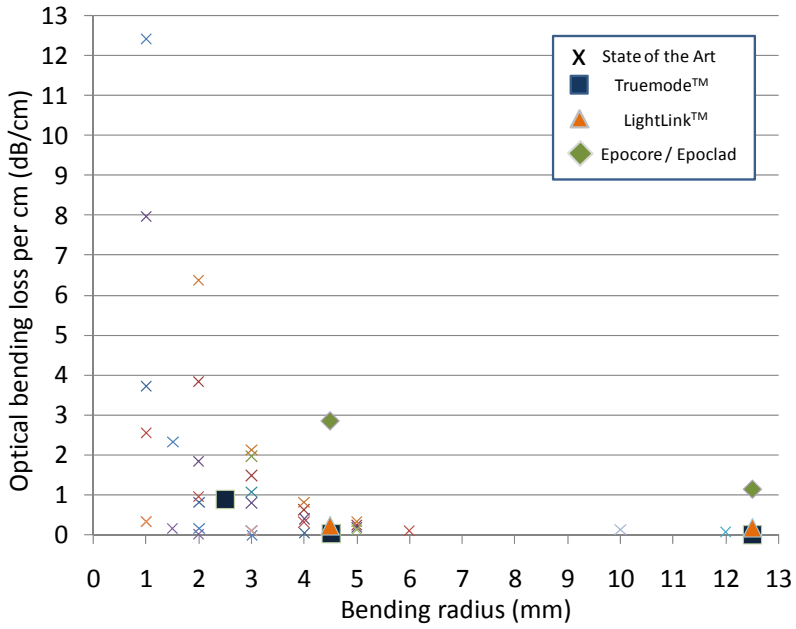

Figure 4.25: Bending losses of Truemode™ Backplane Polymer , LightLink™ and Epocore / Epoclad flexible waveguides versus the bending losses of state-of-the-art flexible waveguides.

which significant improves this poor adhesion. The final waveguide foil however is still very brittle at the waveguide layer side. The application of a top spincoated Polyimide layer had a good influence on the bending behavior of the foil but to a minor extend. Finally, a third approach was investigated showing much better results. Using the principle of the neutral axis, the optical waveguide stack was sandwiched in between two identical spincoated Polyimide layers which were processed in the same process flow as the waveguide stack. The choice of the right Polyimide minimized the CTE and cure temperature mismatch problems. The processing of the waveguide foil is done on a temporary rigid glass carrier, using a selective adhesion promoter deposition and laser ablation combination as release method. The adhesion of Epocore / Epoclad , Ormocers® , Truemode™ Backplane Polymer and LightLink™ with respect to the Polyimide was optimized using plasma etch steps and intermediate adhesion layers. The resulting waveguide foils in these four materials were investigated for their flexibility and optical bending propagation losses. The Truemode™ Backplane Polymer material showed superior bending behavior over the other materials with a minimum bending radius lower than 2.5 mm tested for 1000 bending cycles. The optical propagation losses in the waveguides incorporated with bending are

called the optical bending losses and were measured again for the four materials. The results showed that the Epocore / Epoclad material suffers from very high bending losses, while the LightLink™ and Truemode™ Backplane Polymer bending losses are comparable to those reported in literature. Large Ormocers® waveguide foils (4 inch) could not be fabricated, so no quantification of the losses could be done.

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Chapter 5

Thinning of opto-electronic components

This chapter describes the realization of ultra thin chips (down to 20 μm) by performing a backside mechanical thinning process for individual dies. Within the scope of this thesis, the main interest is dedicated to the thinning of VCSEL and Photodiode arrays, which comprise a GaAs substrate. Mechanical and optical characterization of the chips was performed to confirm their integrity after thinning.

5.1 Introduction

The goal of this thesis comprises the integration of opto-electronic components inside a flexible foil. We choose to work with commercially available components to make this technology more accessible. Standard VCSEL and photodiode arrays are provided with a surface thickness of 150 μm. Embedding of such relatively thick dies together with optical waveguides inside a foil results in some technological problems:

- VCSELs are vertical emitting laser diodes, while the optical interconnection medium is a horizontal waveguide. This introduces the need for an out-of-plane coupling structure on top of the VCSEL. Since the waveguide has a typical height of 50 μm , sandwiched between two cladding layers of 30 μm , the total waveguide stack is already 120 μm thick. Adding the thickness of a 150 μm VCSEL raises the total thickness upto 270 μm . For highly flexible materials, this large vertical dimension does not cause any limitations to the bending of the stack, but most polymers, and especially the polymers used in this work do not show such an excellent flexibility. For acceptable

bending properties, the total thickness of the stack needs to be limited. This is only possible by thinning the embedded dies.

- The flexibility of a system is determined by the flexibility of its most rigid element. In the aim to embed optical interconnections and opto-electronic components inside flexible substrates, the most rigid part are the latter components. 150 μm thick GaAs components are very rigid. If we could thin them down below $\pm$ 30 μm they would actually become bendable. This is taken into account that the dies are embedded in a foil, since bare thin dies are much too brittle and thus fragile to be handled and bended. The flexibility of every component within the foil will also improve the reliability of the system since it is often the flex/rigid interfaces which are the critical failure system in accelerated aging test.

5.2 State of the art: Wafer thinning approaches

A common thickness for standard available electronic chips is 300 μm. Although chip thicknesses downto 100 μm are also in high volume production. This is expected to decrease to about 50 μm in the near future and 20 μm within the next decade [1]. The most efficient way to reduce chip thickness is the thinning of the complete wafer at the back end after the complete device processing on the front side. The state of the art on this topic is mainly driven by the IC industry. As electronics applications shrink in size, integrated circuit (IC) packaged devices must be reduced both in footprint and thickness. The main motivation for the development of smaller packages is the demand for portable communications devices, such as memory cards, smart cards, cellular telephones and portable computing.

This motivation has lead to the development of a series of techniques to backthin Si and other semiconductor wafers. Each thinning process has its advantages and disadvantages. Main qualifying characteristics for a thinning process are removal speed, backside roughness, warpage, cost, yield, and total thickness variation (TTV). The latter is expected to be a main issue since the reduction of the chip thickness is combined with an increasing wafer diameter. Larger wafer diameters require thicker silicon to withstand wafer manufacturing. The requirement of an increasing thickness of the wafers during processing and the contrasting interest of thinner dies makes thinning techniques more and more important. For massive use and production of ultra-thin chips in the IC market, the thickness tolerance is assumed to be 1 μm [1].

5.2.1 Mechanical backlapping

Early report on circuit transfer by backside thinning was made by Hamaguchi et al. [2]. The first step consists of mechanical grinding. This process involves the use of a grinding wheel that rotates while in contact with the backside of the wafer. It is typically used for the removal of bulk material and conducted as a batch process. The main drawback of the grinding process is mechanical damage to the wafer as well as warpage and inhomogenity. This limits the application of grinding in thinning the chip to a certain thickness. Grinding processes are typically used for thinning wafers down to 150 μm , unless special measures are taken. Protection of chips with special layers during grinding is very important. The grinding process however gives the best flatness in the wafer thinning operation [3]. Figure 5.1 compares the total thickness variation (TTV) for etched, polished and grinded GaAs wafers, measured by Skyworks Solutions Inc [4].

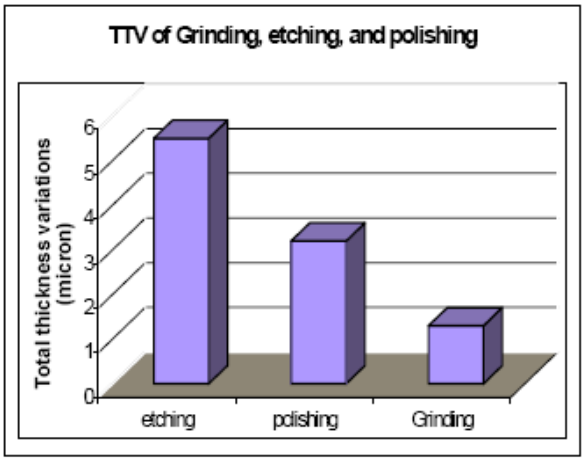

Figure 5.1: Influence of the thinning process on the total thickness variation (TTV)(Source: Skywork Solution Inc.).

A second step of the process is necessary to remove most of the damage layer created by the coarse grinding step and to reduce the surface roughness. Damages induced by mechanical grinding have been analyzed by techniques such as interference contrast microscopy and X-ray topography [5]. X-ray topography has shown that most of the damage is located within a region about 20 μm deep. Defects below this depth probably are point damages not readily resolved by topography. After rough grinding, a complex structure of surface cracks (oriented parallel to 111 directions and about 1 to 2 μm deep in silicon), dislocations are observed. The fine grinding removes most of this layer if standard conditions

are applied (i.e., removal of an additional amount of 20 μm). However, there is a remaining defect band near the surface. The thickness of the defect band is strongly affected by the grinding conditions and is between 0.1 μm and about 1 μm . The residual defects cause stress in the thinned wafer, leading to an additional bow and often broken wafers during handling or further processing. This means that additional thinning is necessary to remove the defect layer.

Skyworks Solutions Inc has proven that the wafer strength is directly related to the surface roughness and that the polishing method had a much better impact on the wafer strength than the wet etching method [4]. Figure 5.2 shows the relationship between backside roughness and wafer strength and its consequences in the handling yield for grinded, polished and wet etched Si wafers (source: [4]).

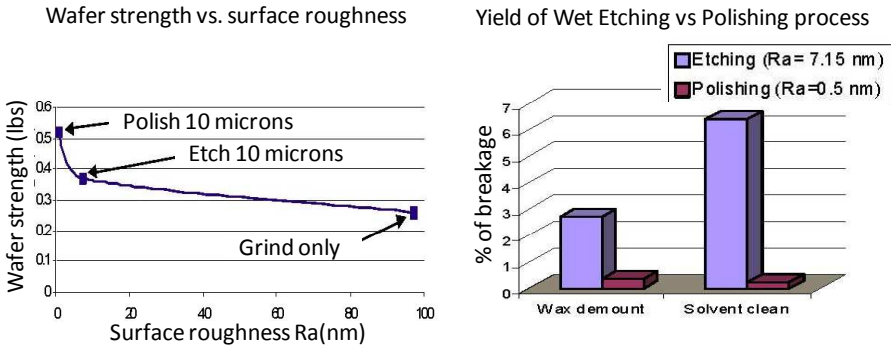

Figure 5.2: Relationship between backside roughness and wafer strength (*left*) and its consequences in the handling yield for grinded, polished and wet etched Si wafers (*right*) (Source: Skywork Solution Inc.).

Because of its high thinning rate, mechanical grinding currently is the most common technique for wafer thinning [6], [7]. All commercially available wafer grinding systems can handle thinning rates of about 5 μm /sec for coarse grinding and about 1 μm /sec for fine grinding or polishing.

GaAs backlapping versus Silicon backlapping

The Department of Integrated Circuit Research and Development in Osaka, Japan reported that the phenomena observed in the back-grinding process for compound semiconductor wafers show considerable differences from those observed with silicon wafers. Most notable is the sudden transition from the high roughness surface phase into the very smooth mirror surface phase. Also notable is that the thickness of the layer deformed by grinding is far thinner than with silicon

wafers. These properties render wafer surfaces free from residual stress through simple chemical etching after grinding [8].

5.2.2 Chemical wet etching

Wet chemical etching is the second most common thinning technique. To etch one side of the wafer, one approach is spin etching, in which a thin stream of an etching agent is moved periodically over the surface of the rotating wafer. The front surface of the wafer is protected either by additional layers or by applying special chucks that allow the processing of thin wafers without surface protection layers or tapes. The benefits of spin-processing technology with its accompanying aqueous chemical etchants can provide increased wafer and die strength, removal of surface damages, crystal defects and micro cracks from backgrinding.
The KarI-Marx-University in Leipzig developed an alternative approach using a vapor jet etching method and suitable equipment in order to thin mono crystalline and polycrystalline material of GaAs, InP and InAs for transmission electron microscopy [9].

	Material Selectivity											
Etchant	GaAs	InP	InGaAs	InGaAsP	GaInP	GaAsP	AlGaP	AlGaAs	AlInP	InAlAs	InGaAlAs	SiO2
$HCL : H_3PO_4$	S	E	S	S	E				E			
$H_3PO_4 : H_2O_2 : H_2O$	E	S	E		S							
$H_2SO_4 : H_2O_2 : H_2O$	E	S	E	E								
$C_6H_8O_7 : H_2O_2$	CD	S	CD					CD		CD		
$HCL : HNO_3 : H_2O$	E	E					E		E			
$HNO_3 : H_2SO_4 : H_2O$	E					E						
$HCL : H_2O_2 : H_2O$	E	E				E						
$HCL : H_2O$	S	E	S						E	CD	CD	
$BHF : H_2O$								CD				E

Legend			
Etches	Selective/Stops	Composition Dependent	No Data
E	S	CD	

Figure 5.3: Material etch selectivity of the different etchant for the common compound semiconductor materials (Source: University of Maryland: Laboratory for Physical Sciences).

The etching agents for silicon are mostly hydrofluoric, nitric acid and acetic acid based mixture (HF and HNO_3). The different mixtures allow different etching rates and are characterized by different selectivity's, which may be important if different layers are involved. Figure 5.3 shows the material etch selectivity of different etchants for the common compound semiconductor materials. A common value for the etching rate for spin etching of silicon is about 10 μm per minute. The TTV value obtained for Si etching depends on the etching time,

but is strongly affected by the flow of the etching agent across the wafer surface. The latter depends on parameters such as wafer rotation speed and motion of the agent stream over the surface. The roughness of spin-etched silicon surfaces is several nm (Rms) and almost comparable to CMP processes [1].

5.2.3 Chemical Mechanical Polishing (CMP)

After grinding, CMP (chemical mechanical polishing) is often an alternative solution for mechanical polishing to remove the defects and smoothen the surface. The thickness control over the entire wafer is one of the critical aspects of this technology. The process is based on buffered silica slurries and is generally used for the polishing of silicon wafers. CMP results in flat surfaces but the thinning rate, however, reaches values of only a few micrometers per minute. The large volume application of the CMP process is optimized for sufficiently thick wafers (about 200 μm or more depending on the wafer size) and is available for thinner wafers only for laboratory use.

5.2.4 Atmospheric Downstream Plasma (ADP) and Dry Chemical Etching (DCE)

Atmospheric downstream plasma (ADP) at ambient pressure has been proposed by Tru-Si Technologies Inc. [10]. The reactant gas is typically CF4. Plasma etching of silicon induces less damage as compared to grinding. A surface roughness Rms of about 0.3 nm was measured for wafers thinned by ADP-DCE. Initially plasma thinning was proposed for the thinning of bond and etch-back of SOI wafers. Plasma thinning can achieve high thickness homogeneity and can thin the top silicon layer down to 1 μm for the as-formed SOI wafers [11]. The drawback is the slow etch rate and the costly equipment [12]. However, the etch rates are at least 100 times higher than can be achieved with vacuum plasmas. In [13],thinning rates of 20 μm /minute and a uniformity $\leq$2 % for removing 20 μm were achieved.

5.2.5 Electromechanical etching

This method is based on the fact that silicon etch rate in some etching solutions is highly dependent on the biasing voltage. For example in HF:HNO3: H2O solutions, selective etch between biased and unbiased regions can be achieved. This technology combines both the bias etching and p/n junction etch-stop. Devices are formed in the n-type region of a p-type silicon wafer. All the areas outside the active region are coated with metal. Then the wafer with devices is glued to a host substrate such as a glass wafer. The backside is then etched in a solution

similar to the ones mentioned in Figure 5.3 . Finally, only the as formed device in the n doped region will be left. However, considering chemical compatibility problems and the rather complex process, this method needs some further development before it can be applied on a large scale.

The University of Texas at Austin applied this thinning process to obtain ultra thin VCSEL arrays out of GaAs bulk wafers, which resulted in highly controlled VCSEL-array thicknesses of 10 μm [14].

5.3 State of the art: Handling of ultra thin chips

5.3.1 Mounting of wafers / dies on temporary carriers before thinning

Thinning wafers to a thickness of 20 μm , makes them enormous fragile and impossible to handle. Therefore the wafers are mounted on a temporary rigid carrier. One mounting approach is the reversible wax bonding. Here the device wafer is coated uniformly with wax and then bonded to a carrier substrate. The use of a carrier substrate allows the application of conventional handling tools during further processing and improves the mechanical strength while the wax reliably bonds and further protects the active surface of the device wafer during thinning. Most of the available waxes, however, are thermally stable up to about 120^{o}C, which is too low for additional thermal processes. As carrier substrates quartz, glass or even Si wafers are commonly used [15]. This type of bonding is termed reversible because device and carrier substrates can be de-bonded quite easily once back thinning has been completed.
Other approaches are the use of a thermoplastic adhesive, or a heat release tape. Liquid thermoplastic adhesives can be applied using a coat and bake step, while dry film adhesives can be applied using a dry film vacuum laminator. Tapes however can no longer be used for ultra-thin wafers. The main reason is the nonuniformity of the tapes.
Maintaining substrate planarity and a tight total thickness variation (TTV) is crucial during wafer-to-carrier mounting, especially when trying to achieve very low target thickness. Liquid spin-on thermoplastic adhesives and waxes tend to offer tight TTV of about 1 μm , although variations do exist depending on the product used.

5.3.2 Dicing of ultra thin wafers

The dicing of ultra thin wafers with standard sawing technologies has offered a range of challenges and problems in the past. To eliminate the influence of

micro-cracks induced by sawing wafers, the Fraunhofer-Institute for Reliability and Microintegration developed a new concept "Dicing by Thinning" [16]. Figure 5.4 shows the principle of the "Dicing by thinning" process.
The concept allows manufacturing of 30 μm thin wafers and includes self acting die separation during the thinning procedure. The process separates the thin and flexible integrated chips by defining a plurality of grooves into the front surface of the wafer to be thinned. Best results are obtained when preparing dry etched chip grooves. The wafer will be thinned until the grooves are exposed. The grooves isolate each IC chip into a separate die. The pre-scribed grooves are typically 50 microns or less. A planarizing and stress-relieving polyimide layer is disposed on the front surface before the grooves are scribed. A low-viscosity low-stress adhesive is disposed on the grooved polyimide coated surface.
Similar dicing concepts were reported by Delft University of Technology [17], and the Microelectronics Stuttgart Institute (IMS-CHIPS) in Germany [18].

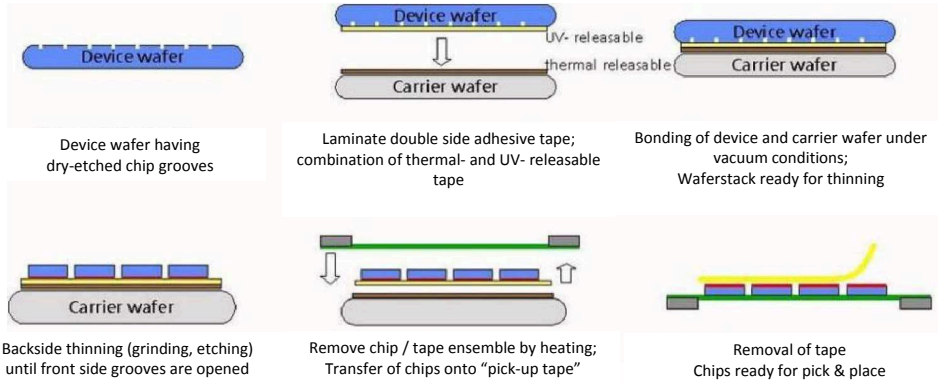

Figure 5.4: Schematic overview of the "dicing by thinning" principle followed by the transfer of the dies from the thinning carrier wafer to a low tac tape (pick &) place tape). (source:IZM)

5.3.3 Handling of ultra thin chips

Handling, mounting, placing of single dies in mass production/assembly processes is often done by vacuum tools, which can pick up the dies from the temporary carrier and mount it on the final substrate by releasing the vacuum. The vacuum chuck, having mostly a smaller diameter than the wafer, is fixed on the front or on the backside. Here, the forced deflection during vacuum sucking is not only increasing by the applied load, but also by the ratio of the wafer diameter to the diameter of the chuck. The deflection increases to the fourth power of both diameters [1]. Therefore, handling systems other than the conventional are

strongly required.
As an alternative, release from the temporary carrier Laser-based direct-write (LDW) processes offers unique advantages to release individual devices from a carrier substrate and transfer them inside a pocket or recess in a receiving substrate using a single UV laser pulse, thus performing the same function as pick-and-place machines currently employed in microelectronics assembly [19]. Figure 5.4 shows a schematic overview of the "dicing by thinning" principle followed by the transfer of the dies from the thinning carrier wafer to a low tac pick & place tape (source:IZM [20]).

5.4 Thinning of individual GaAs chips

The footprint of chips is always minimized to a quite extensive level. The extra cost for chip design is however a tiny concession compared to the cost for a fully manufactured wafer since the process costs for a full GaAs wafer are tremendously high. Therefore whole wafers can contain over 10.000 functional chips. One can ask the question whether the chip thinning process becomes more cost-effective on wafer scale or on chip scale. Is it cheaper to thin every die separately (still in a parallel way) or the whole wafer at once. The answer on this question is adequately hidden in the field of the process yields. Since we cannot have a clear view over the yields of chip thinning so far, this question will remain unanswered for now.
In some cases, thinning of dies is not always possible on wafer scale. Side emitting lasers for example, like any other commercial circuitry or components, first need to be tested on functionality. This kind of devices however does not have the possibility to be tested on wafer scale. They first need be diced and then be measured and tested separately. Testing of these devices when being very thin, is not possible without damaging them. That is why the thinning of individual dies instead of the whole wafer is not optional but absolutely necessary.
Mostly, the choice to thin individual GaAs chips will be driven by the processing throughput. Applications which are in need of very thin GaAs components are very often quite dedicated with a small scale production throughput. Often, there is no need for a full wafer of functional dies. Same can be said for the purchase of chips within the frame of this PhD, where the cost of a complete wafer would be outrageous. In fact, many chip manufacturers do not give access to whole wafers, but only to individual (non-thinned) dies.

S. Pinel et al. [21] reported that individual chips can be thinned down to 10 μm by mechanical lapping when using a specific approach, as schematically illustrated in Figure 5.5. A groove is etched in the carrier wafer. It is slightly larger than the die to be thinned and its depth is a few tens of microns. Then the die is glued into

the groove (Figure 5.5a). Grinding and lapping is performed until the backside of the die is at the same level of the intermediate wafer surface (Figure 5.5b). The dies are then immediately transferred from the grooved temporary substrate to the final substrate by a flip-chip-like mounting step (Figure 5.5 c & d).

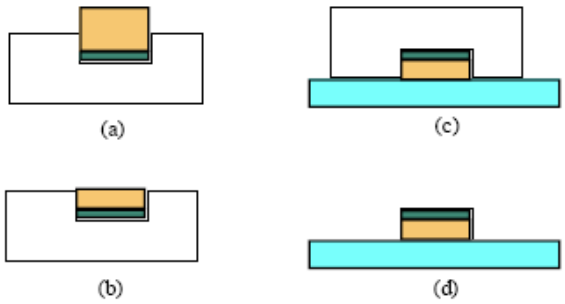

Figure 5.5: Cavity backgrinding approach for thickness control

What follows describes the development and characterization of another process to mount, thin and handle individual GaAs chips without the need of dedicated grooves into the lapping plate. The proposed process is developed in parallel with a process to thin down individual Silicon dies, which is discussed in the PhD work of Wim Christiaens [22].

5.4.1 Set-up

Within the scope of this thesis, a PM5 Lapping & Polishing machine from Logitech Scotland [23] was installed in the cleanrooms of CMST Microsystems. Every work presented in what follows was performed on this machine. Figure 5.6 shows a picture of the PM5 tool as it is installed in the lab.

The principle is as follows: before thinning, the single devices are mounted on rigid glass carriers by means of a mounting wax. These carriers are then fixed on the Jig which holds the glass carrier using a vacuum system. The jig with the glass carrier is placed on a rotating lapping plate. The lapping plate consists of a drive host metal plate, with a top finish of glass, poly-urethane, cast iron or a soft cloth and can rotate with a speed up to 70 rpm. The polishing slurry is located in a dedicated container which rotates to guarantee the uniform distribution of slurry particles within the slurry. A special mechanism guides the slurry from the container to the polishing plate. A screw at the end of the container allows

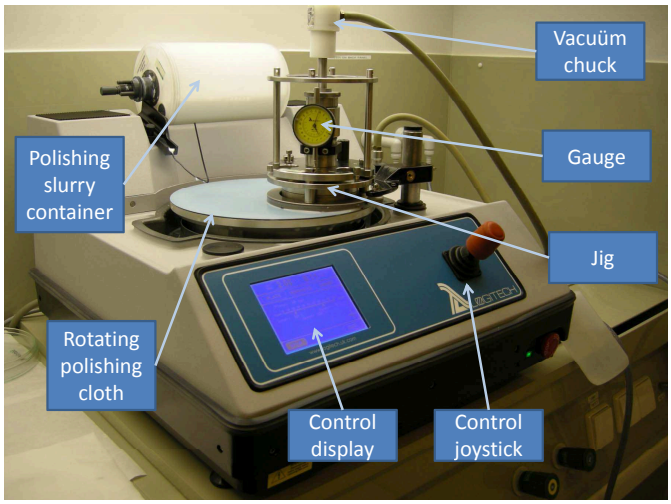

Figure 5.6: Logitech PM5 Precision Lapping & Polishing Machine as installed in the cleanroom

us to control the dispensing speed. A typical speed is one drop per second. The spreading of the slurry drops on the polishing plate is done by a cast iron ring on the Jig, around the glass carrier mentioned above. The Jig itself is fixed into place on top of the polishing plate, but is free to rotate along its vertical axis. Inside the jig, an adjustable spring is included, which presses the chip glass carrier down onto the lapping plate. This way a force of 300 gr to several kilograms can be applied.
Lapping is defined as a process where two surfaces are worn together between a free rolling abrasive. This differs from a grinding or turning process, where the abrasive particle is fixed within the wheel and cuts the material. A consequence of this is that the shape of the lapping plate is constantly changing as the plate wears and will greatly influence the flatness of the piece being lapped. The machine as such is designed to fulfill the parallellism requirements of wafer thinning processes. Therefore, the lapping must be perfectly flat. Since the lapping plate will inherently be also lapped during the process, a periodical adjustment must be made. This is done by polishing the plate with a large block of the same material for a long time. The flatness of the Jig and the chip glass carriers is maintained in a similar way.

5.4.2 Wax Mounting

Before starting the thinning process the dies have to be prepared and fixed, face down, on the 4 inch glass plates. For this temporary bonding on the glass carriers,

wax was chosen. For wafer thinning also lamination of dry film adhesion layers is a viable solution for thin chips ≥ 50 μm . However, the lamination process is not applicable in the case of single dies, since planarization issues will certainly appear. Three different waxes were compared: quartz wax, thin film bonding wax and glycol phtalate (all supplied by Logitech). The melting temperatures are consecutively 90^{o}C, 120^{o}C and 130^{o}C.

Thin film bonding wax Thin film bonding wax is a low viscosity wax which results in a very thin layer of wax of approximately 1 μm . This assures a very thin wax layer underneath the dies, but as experiments have shown, the chip is insufficient protected in this way. The slurry grains will hit on the unprotected side walls of the dies, resulting in the cracking and uncontrolled removal of GaAs fragments. After some time in the lapping process, the dies will be completely crushed. Lowering the load on the dies and the rotation speed did not prevent this to happen. Conclusion: thin film bonding wax is not applicable for small, brittle GaAs dies.

Quartz wax Quartz wax has a higher viscosity and can protect the dies to some degree, but when the dies become thinner than 35 μm , we observe a fatal destruction of the chips. The cause for this behavior is probably found in the hardness of the wax. The incoming forces of slurry grains on the GaAs material are high, especially at the very edges of the dies. As a sort of turbulence occurs at the edges, the wax material will locally become thinner than elsewhere, leaving the die edges unprotected. Complete destruction of the dies is again occurring.

Glycol Phtalate wax Glycol Phtalate wax has an even higher viscosity and covers the 150 μm thick chips right to the top edges, offering chip protection from the very beginning of the lapping process. The hardness of this wax is sufficient to withstand the slurry grain turbulence at the edge of the die, even at thicknesses down to 20 μm . The use of Glycol Phtalate wax has extended the yield of the chip thinning process up to 100 percent (no process failures in 27 different chip thinning runs consisting of mounting, thinning and releasing). The larger wax thickness however asks for special measures concerning the parallellism of the die after wax mounting. Good control over the wax layer thickness underneath the dies is necessary.

Dummies When working with very small, brittle chips like VCSEL and photodiode arrays with dimensions of 1 x 0.3 mm^2, all the applied load of the internal spring in the jig of the PM5 machine is too high and has to be spread over a larger area. The use of dummy chips can bring a solution for this. They are mounted next to the functional chips as is shown in Figure 5.7.

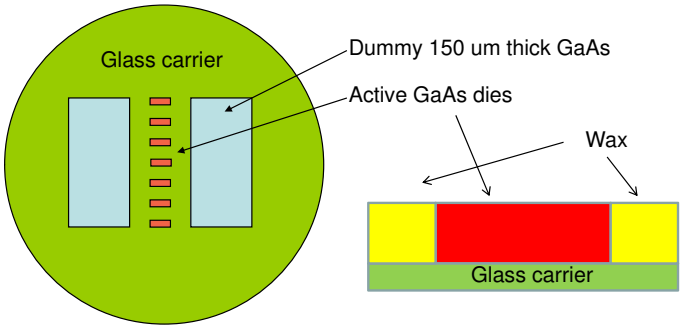

Figure 5.7: Wax mounting on glass carrier of 7 VCSEL arrays with 2 large (2 x 3 mm^2) dummy dies (left) and cross-section (right)

Dimensioning them to about 2 x 4 mm^2 results in a load on the small functional chips which is actually 50 times lower. The positioning of the dummies can contribute to a better distribution of slurry grains in the area of the functional chips and can control the turbulence as well. Obviously, the dummies need to be made of GaAs material and need to be as thick as the functional dies. When they would be thinner, the load would again be only applied on the functional dies. When they would be thicker, the leveling of the dies would be threatened (see below).

Leveling of the chips As mentioned before, a very important parameter in a chip thinning process is the total thickness variation (TTV) of thinned chips, especially when thinning down a chip to a thickness of only 20 μm , since the relative TTV is then even larger. The lapping machine is conditioned to lap down 5 inch wafers with a TTV below 2 μm . The mounting of the dies plays a crucial part in this issue. If the chip is mounted in a tilted way, an additional TTV will be introduced. Therefore we need a good control over the wax layer thickness underneath the chips.

This has been optimized by applying a load of 5 kg on the chips when the wax is above its melting temperature. To release the thickness restraints on the dummy thickness, a pressure redistribution layer is added. In this way, dummy thickness variations may be a few μm , since the foil is compressible. Figure5.8 shows the schematic overview of this technique.

The wax layer thickness is measured for 5 x 5 mm^2 and 10 x 10 mm^2 GaAs dies and shown in Table 5.1. We see that the variation is about 1 μm , which is also the resolution of the measurement tool we used. The variation is below the requirements.

We investigated two different load applying approaches. A first consists of

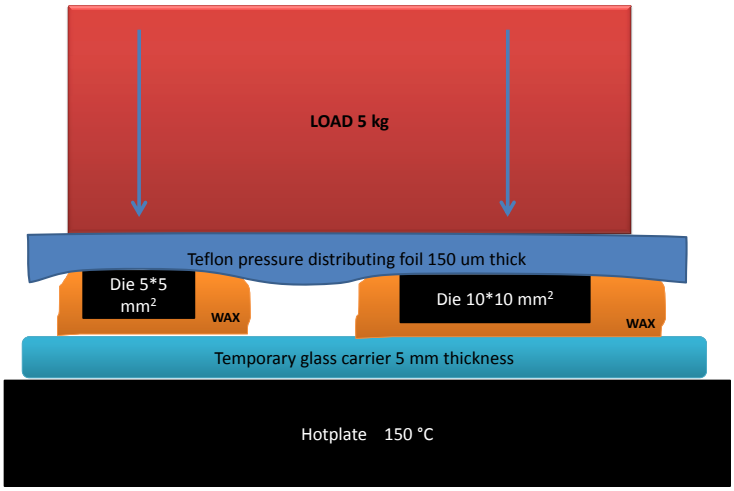

Figure 5.8: Wax mounting of 5 x 5 mm^2 and 10 x 10 mm^2 GaAs dies with the use of a Teflon pressure distribution foil for optimized leveling of the dies after mounting.

Table 5.1: Wax layer thickness underneath the functional dies after wax mounting on temporary glass carrier

Load applying approach	Die dimension	Average wax thickness (μm)	Standard deviation (μm)
during cooling of wax	5 x 5 mm^2	2.6	0.9
during cooling of wax	10 x 10 mm^2	13.0	1.9
during heating of wax	5 x 5 mm^2	2.6	0.9
during heating of wax	10 x 10 mm^2	3.2	1.1

applying the load onto the glass carrier right after it has been removed from the hot plate. This is fast approach since the load will cool the wax and glass carrier down much faster. A second approach is applying the load on the glass carrier when it is still on the hotplate and switch the hotplate off. This is a slow process, since the glass carrier, the load and the hotplate have to cool down together, which can take more than half an hour. The measurements show that for dies of 5 x 5 mm^2 or smaller, we can apply the load when the glass carrier is of the hotplate. This fastens up the process a lot because it takes a long time for the 5 kg load to cool down after 30 minutes at 150^{o}C.

5.4.3 Lapping

Lapping of GaAs chips induces stress and surface damage to the backside. Therefore the thinning process is split into two consecutive steps. the first consists of a lapping process which thins the chips from 150 μm to 50 μm and a second polishing step to remove the damage from the lapping process and thins the chip further towards 20 μm . The parameters of the thinning process were optimized in function of the yield and the qualitative score of the thinned samples. Table 5.2 shows the final parameter set. What follows gives a more detailed description of these parameters and how they were obtained.

Table 5.2: Optimized parameter set for the thinning of GaAs single dies.

Optimized parameters for GaAs lapping	
Equipment	Logitech Scotland PM5
Mounting wax	Glycol Phtalate
Lapping plate material	glass
Lapping slurry	9 μm Al_2O_3 grains in solution
Rotation speed	10 rpm
Applied load	300 g

Lapping plate material A glass lapping plate showed the best results for the thinning of GaAs opto-electronic components. Poly-urethane and soft cloths were also tested, but bad results were found in means of bad parallellism and chip damage. The demand for parallellism is a consequence of the need for a low total thickness variation (TTV) and must be treated with care. The use of a well maintained lapping glass plate results in a high flatness of the chip with a TTV below the resolution of the chip thickness measurement unit ($\leq 1\mu$m).

Lapping slurry material Tests have been performed with Chemlox (provided by Logitect [23]) for chemical-mechanical etching. This kind of slurry is often used for the thinning of GaAs wafers and was recommended by Logitech. However the chemical behavior of the substance is only reacting with the GaAs chip and not with the wax. Since the chemical etching seemed to be more significant than the mechanical lapping, the surface of the chip showed a rounded shape. The thickness in the middle of the chip was about 9 μm lower than the thickness at the edges of the chip, which is unacceptable.
Mechanical lapping with Al_2O_3 grains with a diameter of 9 μm offered the best results.

Rotation speed The rotation speed has, in contrast with what we would expect, a minor influence. Doubling the rotation speed from 10 to 20 rpm does not result

in a double removal rate, but instead, only a 10 percent gain can be obtained. At fast speeds higher than 30 rpm we can also witness more damage to the chip. The material removal rates for different chip sizes is shown in Table 5.3. These rates are high enough for fast processing. Increasing the rotation speed would consequently higher the risk for chip damage. The material removal rate in Table 5.3 for the smallest dies is lower than for the larger dies. This is due to the load spreading over the small dies and the dummy dies mounted next to them.

Table 5.3: Average material removal rate during the lapping process (parameters: see Table5.2)

Die dimension	Material removal rate (μm per minute)
1 x 0.3 mm^2	21.1
5 x 5 mm^2	26.0
10 x 10 mm^2	26.0

Load Similar behavior was measured for the applied load. Raising the load barely raises the removal rate, but an excessive load ($\geq$ 1 kg) results in chip breakage.

5.4.4 Polishing

The parameters of the polishing process were optimized in function of the yield, the backside roughness and backside profile of the thinned samples. Table 5.4 shows the final parameter set. What follows gives a more detailled description of these parameters and how they were obtained.

Table 5.4: Optimized parameter set for the polishing of GaAs single dies.

Optimized parameters for GaAs lapping	
Equipment	Logitech Scotland PM5
Mounting wax	Glycol Phtalate
Polishing plate material	Soft cloth MD-DAC
Polishing slurry	0.3 μm Al_2O_3 grains in solution
Rotation speed	10 rpm
Applied load	300 g

Polishing plate material Polishing on a hard plate like glass or poly-urethane resulted in badly polished dies with lots of larger scratches. The use of a soft cloth for this matter resulted in very good surface roughness's. The soft characteristic of the lapping plate does not guarantee us total flatness, but measurements show

that the TTV is still below the resolution of the thickness measurement unit ($\leq$ 1μm). Figure 5.9 shows the evolution of the thickness of a 5 x 5 mm^2 and 10 x 10 mm^2 GaAs die during the polishing process in each corner of the die and at the center.

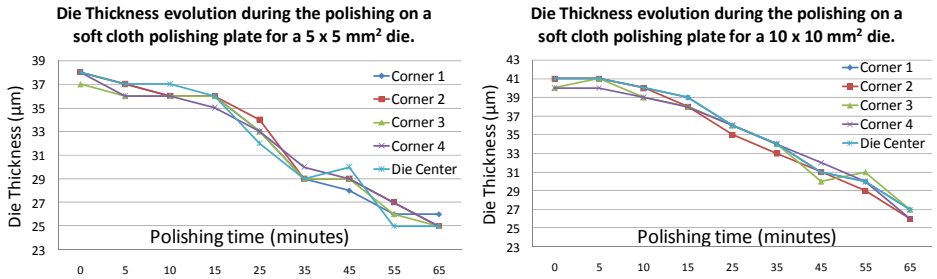

Figure 5.9: Chip thickness evolution during the polishing process for a 5 x 5 mm^2 and 10 x 10 mm^2 GaAs die

Polishing slurry material Chemical solutions as polishing slurry suffer the same disadvantages as they do for the lapping process. A solution of 0.3 μm grains of Al_2O_3 showed the best results.

Rotation speed A very crucial parameter in the polishing process is the rotation speed. With speed exceeding 25 rpm, consistent chip destruction was witnessed. Further research revealed that the problem was situated at the edge of the chips. Next to the edge, a small groove in the wax starts to appear after 5 to 10 minutes of polishing. When polishing further, this groove will become as deep as the thickness of the chip, losing the protection of the side walls of the die. A total crushing of the dies was the result. The lower the rotation speed however, the lower the impact of this phenomenon. It was seen that after 30 minutes of polishing at a rotation speed of only 10 rpm, the wax-grooves next to the die edges were only 1 μm deep. The existence of this grooves induced a slight roundness of the chip edges. Measurements showed that a 1 μm deep groove results in a chip edge roundness of about 0.8 μm . This is shown in Figure 5.10.

Load Raising the load barely raises the removal rate, but an excessive load ($\geq$ 1 kg) results in chip breakage. Doubling the load results in an approximately material removal rate raise of 20 percent. Table 5.5 shows the material removal rates during the polishing process for different chip sizes.

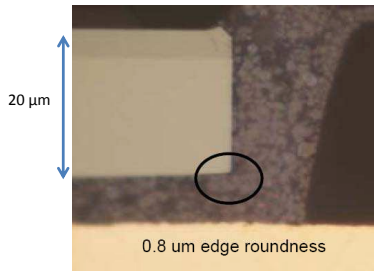

Figure 5.10: Edge roundness of a thinned VCSEL array due to the grooves in the wax at the edges of the die

Table 5.5: Average material removal rate during the polishing process (parameters: see Table5.4)

Die dimension	Material removal rate (μm per minute)
1 x 0.3 mm^2	0.41
5 x 5 mm^2	0.21
10 x 10 mm^2	0.19

5.5 Characterization of ultra thin GaAs chips

5.5.1 Mechanical characterization

The mechanical characterization of thinned chips consists mainly of the visual inspection of the thinned die and the quantification of the backside roughness. Actual bending properties of these thin chips can only by examined when they are packaged in a foil. This is described more in detail in Section 4.7 in Chapter 4. In this section we separate the mechanical characterization of GaAs chips in large and small dimension dies.

Thinned VCSEL and photodiode arrays

The specifications of the opto-electronic components which are thinned and described in what follows, are shown in Table 5.6

Figure 5.11 shows pictures from thinned VCSEL and Photodiode arrays in non-thinned status (150 μm) and thinned down to 35 μm and 20 μm. No visual damage on the top face of the dies can be seen on a regular microscope after thinning.

For massive production of ultra thin chips in the IC market, the thickness tolerance is assumed to be 1 μm . Figure 5.12 shows the backside profile measurement with a non-contact profilometer WYKO of a lapped (left) and a polished (right)

Table 5.6: Specifications of the investigated opto-electronic components.

1 x 4 VCSEL array ULM850-05-TT-C0104U	
Provider	ULM Photonics [24]
Width & Length	350 x 1000 μm ^{2}
Thickness	150 μm
Contacts	Top-Top
Emission wavelength	850 $\pm$ 10 nm
Threshold voltage	1.7 $\pm$ 0.2 V
Optical output power	1.5 $\pm$ mW
Slope efficiency	0.4 $\pm$ 0.1 W/A
Beam divergence	20^o
3 dB modulation bandwidth	3 GhZ
1 x 4 Photodiode array PDCA04-70-GS	
Provider	Albis Optoelectronics AG [25]
Width & Length	450 x 1000 μm ^{2}
Thickness	150 μm
Contacts	Top-Top
Responsitivity (λ = 830 - 860 nm)	0.6 A/W
Diameter of aperture	70 μm
Dark current (T = 25^oC)	1 nA
Bandwidth	10 Ghz
Bias voltage	2V

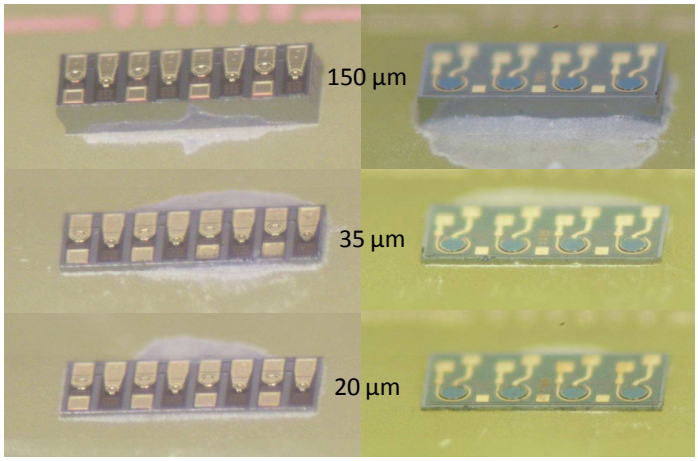

Figure 5.11: VCSEL arrays (left) and Photodiode arrays (right) in non-thinned status (top) and after lapping and polishing (center and bottom)

1 x 4 VCSEL array. A thickness variation of 1.6 μm over the whole chip can be observed after polishing (see Fig.5.13), which is near the mass production tolerances. This thickness variation may not be confused with the edge roundness discussed in Subsection 5.4.4. Figure 5.13 shows the thickness profiles over the length and width axis of the VCSEL array after polishing.

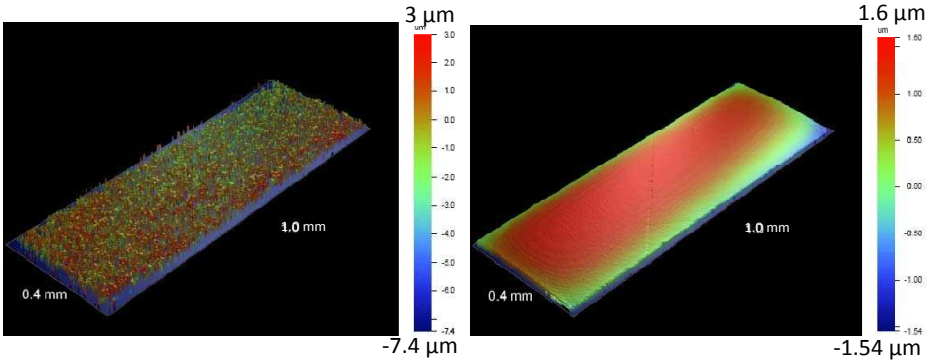

Figure 5.12: Backside profile measurement with a non-contact profilometer WYKO of a lapped (left) and a polished (right) 1 x 4 VCSEL array

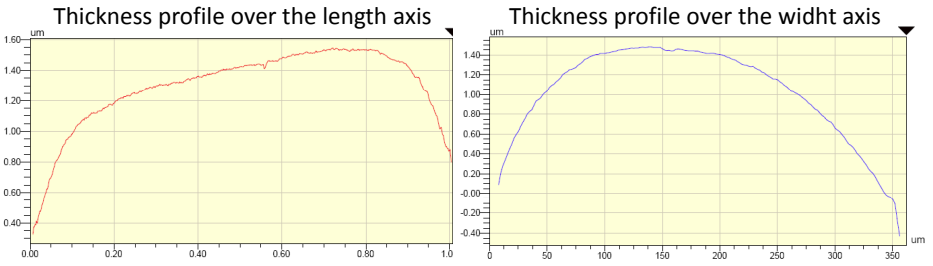

Figure 5.13: Thickness profile over the length and width axis of a polished 1 x 4 VCSEL array

The chip strength is directly related to the surface roughness of the backside [4]. Backside roughness induces micro-cracks and internal stress which is even more significant when the thin dies will be bent, so minimized roughness is preferred. In Section 5.2.1 of this chapter we depicted that the stress inside a GaAs chip after lapping is expected to be very low in GaAs chips, compared to Silicon chips. The presence of possible micro-cracks however still demands for a low roughness chip backside. Figure 5.14 shows a backside roughness measurement with a non-contact profilometer WYKO of a lapped (left) and a polished (right) 1 x 4 VCSEL

array on an area of 200 x 200 μm ^{2}. After polishing, an Rms roughness of 10 nm is measured at the backside, resulting in a very smooth surface.

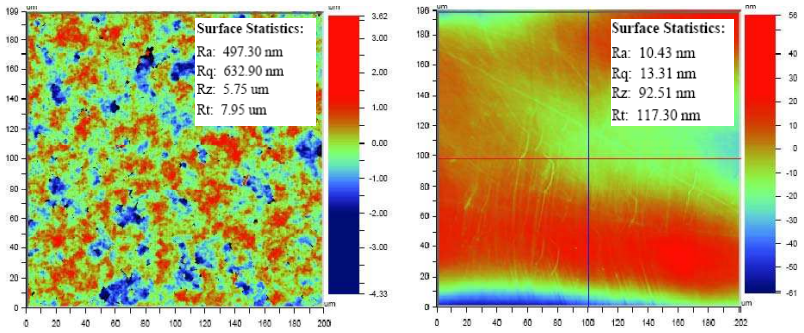

Figure 5.14: Backside roughness measurement with a non-contact profilometer (WYKO) of a lapped (left) and a polished (right) 1 x 4 VCSEL array

To detect any internal cracks, a cross-section of an embedded lapped and polished VCSEL array was fabricated and examined with a microscope (100X magnification). Multiple cross-sections on the same embedded chip were made to be able to "scan" the internal structure of the VCSEL. No visual internal damage can be found on any place of the cross-section. Figure 5.15 shows a picture of such a cross-section and 2 close-ups.

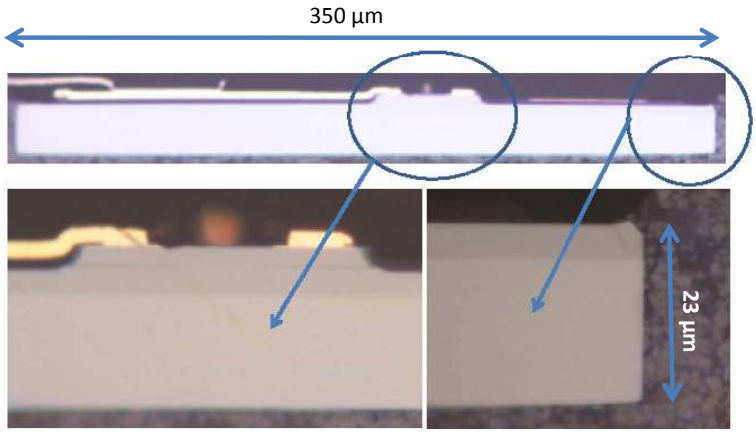

Figure 5.15: Cross-section of a lapped and polished VCSEL array and close-ups.

Thinned large GaAs dies

The thinning of VCSEL's and photodiodes is a very important procedure for this thesis, but these chips are only a marginal part of the GaAs chips available on the market. Their size is so small that the lapping side effects at the edges of the dies are actually overlapping each other. To qualify the thinning process as a complete technique for single die thinning, one must look at the possibility to scale this process to larger dies. What follows describes the mechanical characterization of 5 x 5 mm^2 and 10 x 10 mm^2 dies. The used process parameters are the same as for the small dies and are explained in section 5.4.3 and 5.4.4.

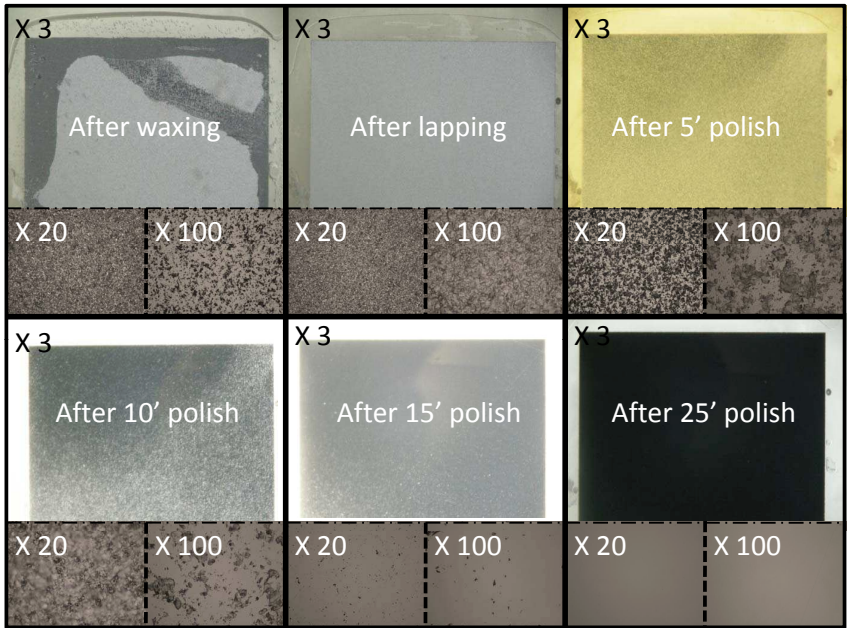

Figure 5.16: Backside roughness pictures for a 10 x 10 mm^2 GaAs die during the different thinning steps with magnification 3X, 20X and 100X

Lapping times for larger dies are similar to the small dies (see: Section 5.4.3). Main difference are the longer polishing times due to the lower removal rate (see: section 5.4.4). Figure 5.16 shows pictures of the backside roughness for a 10 x 10 mm^2 GaAs die during the different thinning steps with magnification 3X, 20X and 100X. In the first picture is shown that the wax can be on top of the die after wax mounting, but this has no effect on the uniformity and on the thickness of the wax layer underneath the die. The amount of surface damage after lapping can be well compared to the surface damage in the original 150 μm status, which

could mean that the purchased GaAs die was also thinned (probably from 500 μm to 150 μm) using the same thinning process and grain size but on wafer scale. After a polishing time of 25 minutes, we can see that the main roughness of the lapping process has disappeared. Considering a material removal rate of 0.19 μm per minute, we have removed 4.75 μm after 25 minutes. This does not mean however, that the polishing process may be stopped after 25 minutes. The depth of the lapping damage is determined by the deepest groove over the whole die, which is most probably deeper than 4.75 μm . When considering large scale processing, one must also build in a safety margin. The sum of all factors named here can add up to about 20 μm, which is the proposed polishing depth in section 5.2.1.

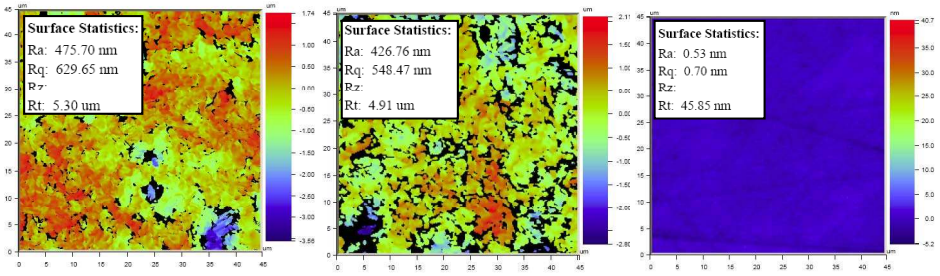

Figure 5.17: Non contact profilometer (WYKO) roughness measurements of a 10 x 10 mm^2 GaAs die on an area of 50 x 50 μm ^{2}. Left: not thinned; center: after lapping ; right: after 65 minutes polishing

Figure 5.17 shows WYKO roughness measurements of a 10 x 10 mm^2 GaAs die on an area of 50 x 50 μm ^{2} for a non-thinned die (*left*), a lapped die (*center*) and a polished die for 65 minutes (*right*). We can again see the similarity between the unlapped and the lapped die backside roughness. The final rms (root mean square) roughness of the GaAs die after 65 minutes polishing and thus the removal of 12 μm , is below 1 nm, which is a much lower value than the roughness measured on a VCSEL or photodiode array (10 nm, see section 5.5.1). The measurement for the small dies was done on a larger area (200 x 200 μm ^{2}), which result in a slighter higher rms roughness value. This is however not the main reason for this roughness difference. When we repeat the measurement on the large die, but on the edge of the chip instead of somewhere in the middle, we see a an additional roughness of about 5 nm. The explanation can be found in the interface between the chip and the wax at the edges of the die. Slurry grains arriving at a certain speed at this interface can be deflected and can perform higher pressure on the GaAs resulting in slightly deeper grooves. In the middle of the die, there are no interfaces, just plain GaAs, resulting in a very uniform distribution of material removal and a very low rms roughness below 1 nm.

At the very edge of a thinned large GaAs die, a major problem was encountered. Small pieces of GaAs were ripped of the die, despite the hard wax protecting it, see Figure 5.18. This edge damage does not exceed a strip of 13 μm along the edge. This problem does not appear with small dies. Further research to find the reason behind this issue did not result in any clarity. One possible reason, however not scientifically proven, is that the large dies were diced by us and the small dies were diced by the VCSEL and photodiode providers. A difference in edge stress and micro cracks could be the case. Placing dummies all around the functional die resolves this problem but extends the complexity of the mounting process. Figure 5.18 (bottom) shows the edges of the 10 x 10 mm^2 dies which were thinned down using the surrounding dummy technique. Edge damage was limited below 1 μm as was also the case with the small GaAs dies.

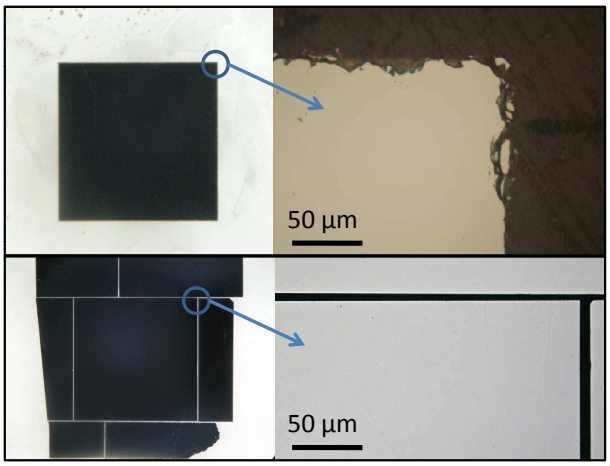

Figure 5.18: Edge damage after thinning of large GaAs dies (10 x 10 mm^2) without the use of dummies (top) and with the use dummies (bottom).

5.5.2 Electrical characterization

Major electrical characteristics of diodes are included in the I/V curve. Figure 5.19 shows the measured I/V curves of 4 different VCSEL's before and after thinning. The curves are almost overlapping and are slightly shifted from each other. The shift tends to be in an arbitrary direction, meaning this is only a result from the measurement tool resolution. Between two separate VCSEL's we see a much larger shift in the I/V graphs. This is however expected since every VCSEL inherently differs from the others, even when fabricated in the same run and even positioned on the same VCSEL array, like it was the case in this measurement.

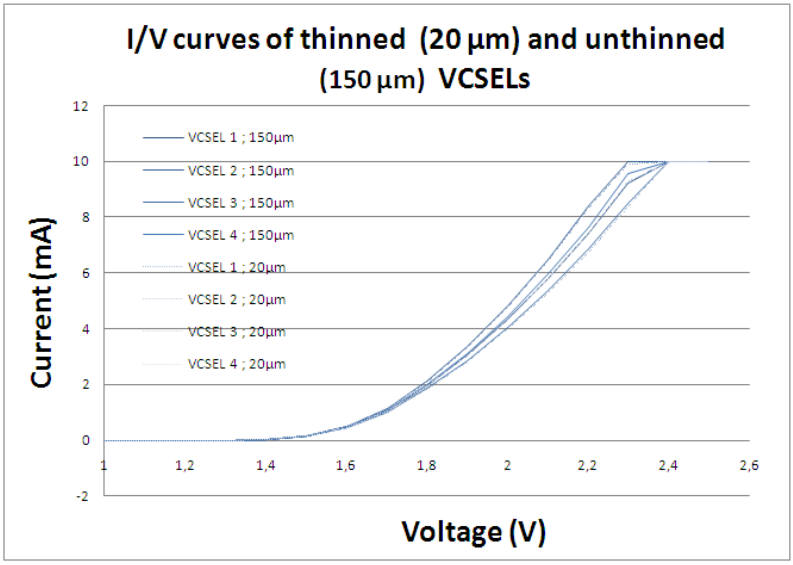

Figure 5.19: I/V Curves of 4 different VCSEL's in unthinned (150 μm) and in thinned (20 μm) status

5.5.3 Optical characterization

The optical characteristics of a VCSEL are legio (emission wavelength, threshold current, optical output power, slope efficiency, 3 dB modulation threshold, rise and fall time, spectral bandwidth, beam divergence, etc...). The thinning process does not change anything to the structure of the VCSEL except from the internal stress to some extent, so no changes in characteristics is expected. In literature it is believed that the thinning by lapping, followed by a polishing step will even eliminate additional stress (see section 5.2.1). The thinning of VCSEL's and photodiodes to a thickness of 20 μm (which makes them physically bendable) has never been done to our knowledge. Therefore it is necessary to compare the behavior of a thinned and unthinned VCSEL. Measuring all the optical parameters (few listed above) would be very time consuming, so a well considered choice of parameters must be made.
The measurements shown below have been done in close cooperation with the research Group "Vakgroep Toegepaste Natuurkunde & Fotonica TONA - TW Faculteit Toegepaste Wetenschappen - Vrije Universiteit Brussel".

Measurement sample To be able to monitor the optical behavior, we need to mount the VCSEL and connect it electrically. A simple concept package was cre-

ated by gluing the VCSEL to an FR-4 printed circuit board, provided with copper interconnection tracks and wirebond the VCSEL to these tracks. To enhance the adhesion of the wire bond, a nickel-gold finish was applied on top of the FR-4 tracks. Figure 5.20 shows such a wire bonded VCSEL package. The tails of the wire bonds were removed manually so they do not interfere with the optical path.

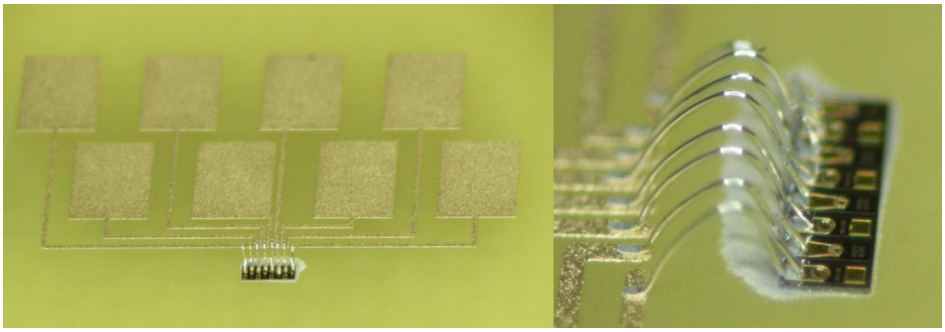

Figure 5.20: Wire bonded VCSEL package for optical characterization of a thinned VCSEL

Measurement set-up The sample as such is mounted on an optical measurement set-up as shown in Figure 5.21. The light coming out of the VCSEL is focused with a lens (focal length of 35mm) and deflected by 45 degree mirror to a coupler unit. This latter component couples the light into a fiber, which guides the light to either a powermeter (Newport Dual Channel Power meter) or an optical spectrum analyzer (OSA AQ6317B). Labview was used for a semi-automatic detection of power peaks in the optical spectrum.

Mode appearance threshold Nearly all VCSEL's in use for data communications are multitransverse mode lasers (MTM) and more specific, MTM oxide VCSEL's are the workhorse in this application area. They are most utilized because they offer modulation improvements over a proton VCSEL, and reliability improvement over a single mode VCSEL. They can be made to be compatible with driving electronics and inexpensive optical coupling. A MTM oxide VCSEL allows more than one optical mode inside the laser cavity. The addition of the oxidation boundary introduces a significant optical effect into the VCSEL cavity. As a result, modes are often more predictable. Figure 5.22 shows the near field profiles of two oxide aperture VCSEL's for increasing diver current [26] (the VCSEL's used in this thesis are oxide aperture VCSEL's). At low driver currents (around the threshold), only one or two modes are visible, while at 5 mA already 5-7 modes are visible. At even higher currents, the modes can barely be separated

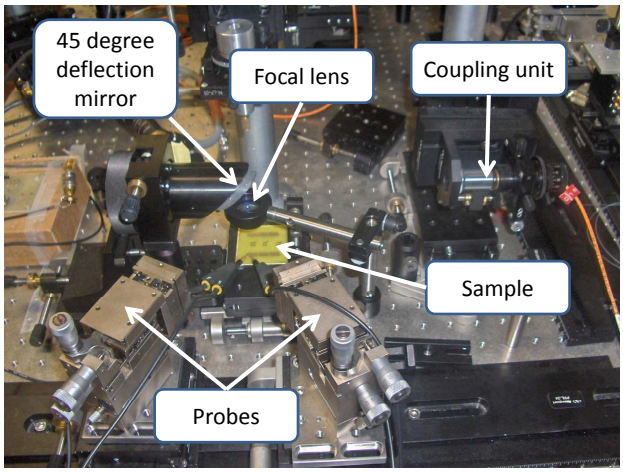

Figure 5.21: Optical measurement set-up for the characterization of thinned VCSELs

from each other. The existence of specific modes is thus subject to the driver current in the VCSEL.

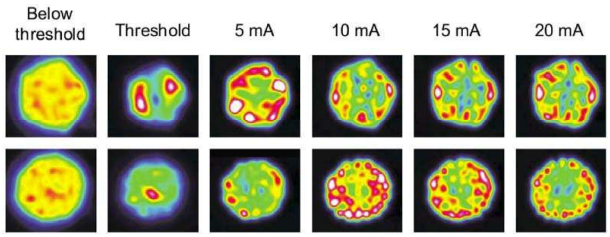

Figure 5.22: Near field images of 2 different oxide VCSELs for increasing diver current (Source: Finisar Corporation).

To map the optical output of the VCSEL, we can look at its optical spectrum for a certain range of driver currents, unravel all the mode peaks and quantify them by their peak power. This way we can actually obtain a "mode fingerprint" of each VCSEL (VCSEL also have a polarization fingerprint [27]). With this in mind, we can start to compare the VCSEL fingerprints of thinned and unthinned, packaged and unpackaged, bent and unbent VCSEL's. In this section we only focus on the comparison of thinned and non-thinned VCSEL's. For example: Figure 5.23 shows the optical spectrum of a non-thinned VCSEL driven with a current of 3.7 mA. More than nine peaks are clearly visible. The peaks have a peak power of (from left to right) 0.08 0.24 0.27 0.42 0.58 0.81 0.95 1.08 and 2.25 mW.

Repeating these measurements for drivers currents ranging from 0 to 5 mA with

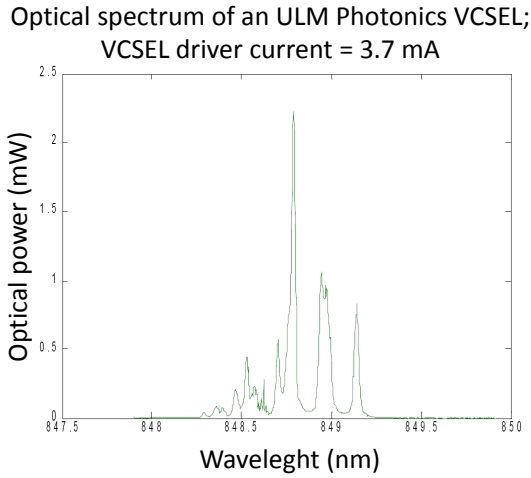

Figure 5.23: Optical spectrum of an unthinned ULM Photonics VCSEL, driven with a current of 3.7 mA.

a 0.1 mA interval results in the graph in Figure 5.24, where every peak is represented by another color as depicted in the graph legend. The power peaks summed up above at 3.7 mA can also be retrieved from this graph. Below the threshold current of 0.7 mA, the VCSEL does not emit any light. Between 0.7 mA and 1 mA the multimode VCSEL functions as a mono-mode VCSEL, however close to the 1 mA threshold, mode jumping with the second mode could occur and use of the VCSEL as a mono-mode light source should be handled with care.

Figure 5.25 shows an overview of the driver current mode appearance threshold of the first 7 modes for a 150 μm , 50 μm and 30 μm thick VCSEL. The identification number of a mode deflects the chronological order in which this mode appears when increasing the driver current. We see that the three graphs are very similar with equal mode appearance thresholds for the different modes, which lets us conclude that the lapping neither the polishing of the VCSEL induces any change in optical behavior of the VCSEL.

5.6 Conclusions

The thinning of Si and GaAS wafers is a widely applied process using many different techniques. The thinning of individual GaAs by mechanical backside lapping and polishing is however never reported. A process flow was optimized to thin down VCSEL and photodiode arrays to a thickness of only 20 μm . Consecutive lapping and polishing steps are developed, resulting in a high yield process.

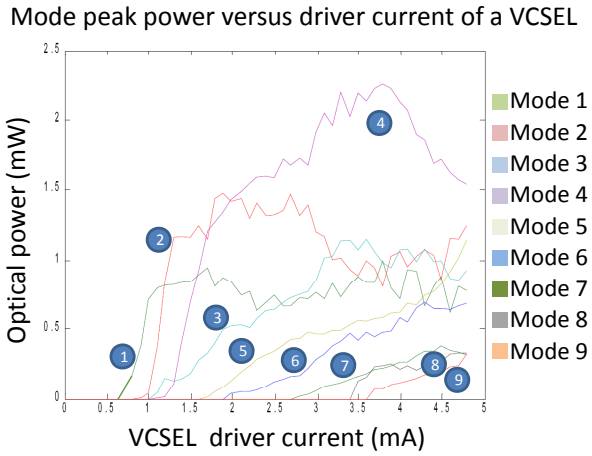

Figure 5.24: Power of each mode peak in the optical spectrum emitted by a multimode VCSEL versus the driver current.

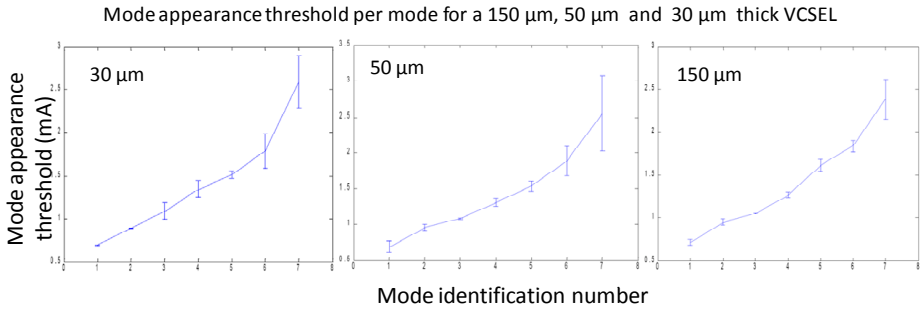

Figure 5.25: Mode appearance threshold per mode for a 150 μm , 50 μm and 30 μm thick VCSEL

Mechanical stress inside the GaAS dies was minimized by reducing the backside roughness to 10 nm rms, measured in an area of 200 x 200 μm^2. Before thinning, the dies are wax-mounted onto a temporary carrier. The flatness of the final thinned dies is below 2 μm due to the optimization of the wax-mounting and the lapping tool maintenance. The scalability of the thinning process to larger chips with dimensions 5 x 5 mm^2 and 10 x 10 mm^2 is demonstrated with an rms backside roughness below 1 nm in the die center. The problem of edge damage with these larger dies was solved by the use of dummies. Electrical and optical characterization of thinned VCSEL's showed that the removal of the backside substrate does not affect its functional behavior.

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Chapter 6

Embedding of actives in the optical waveguide foil

This chapter describes the research to accomplish embedding of ultra thin opto-electronic components like VCSEL's, photodetectors and electronics inside the optical waveguide foil developed in Chapter 4. The thinning of the components is described in Chapter 5. The embedding of these ultra thin actives inside the polymer waveguide stack demands for the fabrication of heat sinks, laser ablated cavities and electrical interconnection features like micro-via's and embedded copper tracks. The fabrication and characterization of all these features is discussed in detail in this chapter.

6.1 Introduction

The flexible waveguide foil developed in Chapter 4 can be used as a flexible optical wire and functions as a pure transmission medium. Passive functionalities could be added to the foil by implementing splitter and multiplexer structures applied on the waveguides. This results in optical re-routing applications in complex opto-electronic systems. In all cases, the active functionality (optical sources, optical detectors, electrical IC's, drivers, etc.) is still assembled on rigid boards, which encloses the electrical routing and thermal management of the actives. Mounting and aligning the foil on to these rigid boards introduces extra difficulties and cost and the flexible character of the system is lost. The goal of the work described in this chapter is the embedding and integration of these actives and their accompanying features inside the flexible optical waveguide foil. With this realization, the waveguide foil becomes a stand-alone active foil with optical as well as electrical functionalities which has the great advantage to be flexible and very compact.

When embedding actives, one need to include extra features for the electrical connectorization since the classical flip-chip and wire bond methods are not always compatible. The fabrication and metallization of electrical via's is discussed in detail in this chapter, together with the embedding of electrical copper fan-outs to larger contact pads. The embedded contact pads are then later opened by laser ablation of the contact pad covering polymer.

Actives can produce a lot of heat when functioning, which can be detrimental for the reliability and lifetime of the system if not spread sufficiently. The heat management of embedded dies is described more in detail in Chapter 8, but in this chapter we mainly focus on the fabrication of heat sinks and on the compatibility of the process flow with larger heat distributing components if necessary. In the complete process of realizing an active embedded optical waveguide foil, the presence of heat and the possibilities to spread it are being kept in mind.

6.2 Embedding of ultra thin opto-electronics

Figure 6.1 shows the schematic overview of the process flow to embed ultra thin opto-electronics. For reasons which will be explained later in Section 6.4, the embedding material is SU-8 from MicroChem Corporation [1]. The embedding of the dies was realized on rigid as well as on flexible substrates. The embedding process is however always performed in rigid status, meaning that in case of a flexible substrate, this latter is mounted on a temporary rigid carrier as depicted in Section 4.6.1, Chapter 4. The different steps of the embedding process flow are described in what follows.

6.2.1 Heat sink

Active opto-electronic components as VCSEL's are known to produce a lot of heat when functioning. This heat can only be spread in the surrounding polymer material, which has an inherent low thermal conductance typical for almost all polymer families. For this reason, extra measures need to be taken to tackle the heat accumulation. Underneath the active, we provide a copper heat sink island which will act as a passive heat spreader. The characterization and optimization of the dimensions of these heat sinks is discussed in detail in Chapter 8, Section 8.6. In this Chapter, we will limit the discussion on the actual fabrication of the heat sink, knowing that the presented heat sink fabrication is scalable in X,Y and Z dimensions.

For the embedding of dies on a rigid substrate, we start from an FR-4 substrate

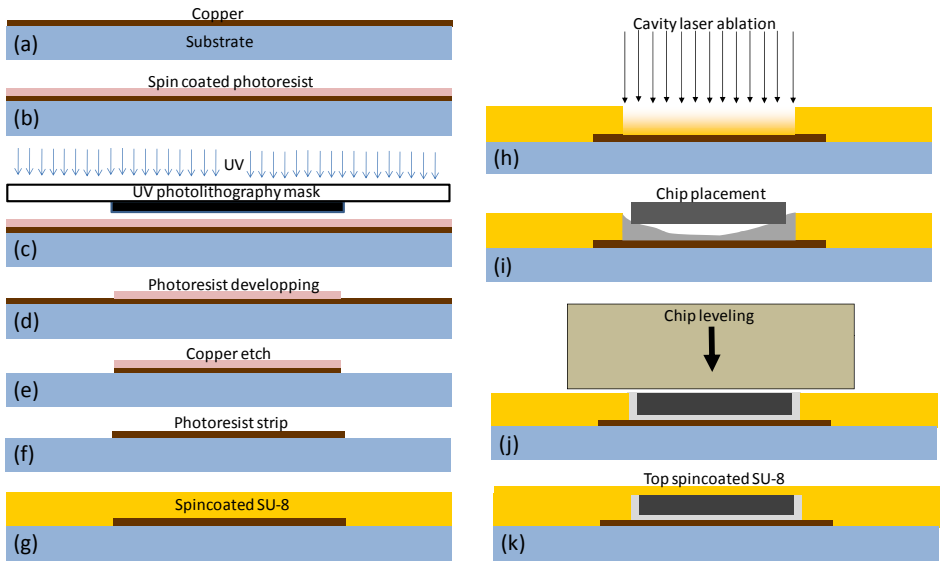


Figure 6.1: Process flow for the embedding of ultra thin opto-electronics in SU-8 material

with a 17 μm thick copper coating (Fig 6.1(a)). An AZ4562 photoresist layer [2] with a thickness of $\pm$ 9 μm is spincoated on top of this copper layer (Fig 6.1(b)). This layer is selectively UV-exposed during photolithography (Fig 6.1(c)) and consecutively developed (Fig 6.1(d)). After development, only the areas of the heat sink islands are covered with photoresist. Table 6.1 shows the process parameters for these steps. After hardbake of the photoresist, the uncovered copper is removed by an etching process (Fig 6.1(e)). The etchant fluid consists of:

- 300 gr Copper-chloride ($CuCl_2$)
- 300 ml HCl
- 600 ml DI-water

With this constitution, the etchant reaches an etching rate of 6 μm /minute, which means that the etch time is only 3 minutes. The resolution of this process is rather limited but the copper heat sink islands have dimensions of several square millimeters, so a low resolution is no draw-back. The etching is done while stirring the etchant for optimum etch uniformity. After etching, the photoresist which is still on the heat sinks is removed in a stripping process consisting of a consecutively 2 minutes Acetone bath strip, a 2 minutes Acetone/IPA bath strip and an IPA rinse (Fig 6.1(f)).

Table 6.1: Process steps and process parameters for the photoresist deposition on the designated copper heat sink islands.

AZ4562 photoresist deposition process.	
Process step	Process parameters
Room temperature conditioning	take photoresist out of fridge for 1 hour before processing
Spin coat	2000 rpm ; 40s
Prebake	90 ^{o}C; 3 min.
UV mask exposure	22.5 s ; 10 mW/cm^2
Development	60s ; MicroDev developer
Hard bake	30 min. ; 120 ^{o}C

For the embedding of dies on a flexible substrate, we cannot start from a copper coated substrate, since we spincoat the flexible Polyimide substrate. Therefore we need additional metal coating steps. The adhesion of the copper to the Polyimide needs to be optimized since the Polyimide is chemically inert. Two plasma etch steps are needed to enhance the metal adhesion. The parameters for this plasma treatment are optimized in the framework of other research projects and are shown in Table 6.2.

Table 6.2: Optimal oxygen plasma parameters of Polyimide layers to enhance the adhesion with metal layers.

Gas 1	Flow 1 (scmm)	Gas 2	Flow 2 (scmm)	Power (W)	Pressure (mTorr)	Duration (min.)
CHF_3	5.0	O_2	20	150	100	2
CHF_3	0	O_2	25	100	150	2

A seed copper layer of 1 μm is deposited on the treated Polyimide layer by means of a sputter process with an Alcatel SCM600 sputter device. A very thin TiW layer of 50 nm is sputtered first to act as an adhesion promoting intermediate metal layer for optimum adhesion (see the peel strength tests in Figure 6.14 in Section 6.4.2). The sputter parameters are shown in Table 6.3.

The sputtered copper layer is than thickened to $\pm$ 10 μm by electroplating. The electroplating parameters are shown in Table 6.4. The micro-etch step cleans the copper seed layer from oxidation and actives the surface for the plating. The anti tarnishing step protects the finished plated Cu layer from oxidation to some extend and the post plating bake takes care of the hydrogen relief after plating.

The thickness uniformity of the electroplated copper layer is dependent on the anode set-up and the electrolyte's homogeneity. A simple measurement of the thickness distribution over the whole substrate shows us that the obtained aver-

Table 6.3: Sputter parameters for the deposition of a 50 nm thick TiW layer and a 1 μm thick Copper layer.

50 nm TiW / 1 μm Cu Sputter parameters			
Process step	TiW	Cu	unit
Starting vacuum pressure	4.10^{-7}	4.10^{-7}	mbar
Substrate rotating speed	10	10	rpm
Flow Argon	$\pm$30	$\pm$24	sccm
Argon pressure	10^{-2}	5.10^{-3}	mbar
Pre-sputter time	1	1	min.
Layer thickness	$\pm$ 50	$\pm$ 1000	nm
Sputter time	100	600	s
Power	1200	2000	W
Voltage	360	470	V
Current	2.9	3.9	A

Table 6.4: Electroplating parameters for the deposition of $\pm$ 9 μm copper on top of a 1 μm thick sputtered copper layer on a 2 x 2 square inch substrate.

Electroplating of 9 μm copper on top of a 1 μm sputtered Cu layer	
Process step	Process parameters
Micro-etch	40 s in sulfuric acid bath
Electroplating	37 min. / 1.5 A/dm^2 / standard electrolyte solution
Anti tarnishing	3 min. in Cuprotec 3 bath
Post plating bake	60 min. @ 110 ^{o}C

age copper thickness is 9.5 μm with a standard deviation of 0.9 μm , all within an acceptable value.

6.2.2 SU-8 embedding layer

As mentioned above, the embedding material for the ultra thin opto-electronics is chosen to be SU-8. The use of Ormocers® , LightLink™ and Epocore / Epoclad have some problems which are difficult to overcome as will be described in Section 6.6. The use of Truemode™ Backplane Polymer as embedding material has only one problem, which could be solved, but this is explained more in detail in Section 6.4.3. Therefore we will focus on SU-8 as material for what follows in this section.

Different versions of SU-8 materials were investigated: SU-8 2050, SU-8 50 and SU-8 10. The first two are developed to realize layers with a minimal thickness of 50 μm . The fabrication of a single layer with these two versions however shows

some serious air-bubble insertion problems. Even if the trapped air bubbles are invisible after spinning, they will appear during the pre-bake steps, making the layer totally unuseful. By putting the bottle of SU-8 material at an elevated temperature of 50 ^{o}C for a whole night, we can reduce the amount of air bubbles but were not able to eliminate them. The problem is more significant for the SU-8 2050 version than for the SU-8 50 version. The SU8-10 material does not show this behavior. If for any reason, an air bubble is inserted in the layer after spin coating, the air bubbles disappear during the prebake steps, resulting in a very nice smooth air-bubble-free layer. The layer thickness obtained for this SU-8 material are shown in Table 6.5 for different set-ups.

Table 6.5: SU-8 10 layer thicknesses for different set-ups

SU8-10 layer thickness		
Set-up	Spinspeed (rpm)	Layer thickness
1 layer on top of other SU-8 10 layer	1000	29 μm $\pm$ 1.8 μm
2 layers on 17 μm thick copper island	1250	35 μm $\pm$ 2.1 μm
2 layers on 17 μm thick copper island	1250 and 1500	28 μm $\pm$ 2.0 μm

The optimized process flow to obtain an 28 μm thick SU8-10 layer on top of a 17 μm thick copper island is given in Table 6.6. The reason for this ideal thickness of 28 μm is explained later on in this section.

The resulting substrate progression at this stage is shown schematically in Fig. 6.1(g).

6.2.3 Laser ablated cavity

Integrating discrete components like opto-electronics creates non-uniformities and steps in the layer build-up, while we would benefit from an optimized planarization. The solution to this, is the use of cavities. When putting the discrete component inside the cavities, the above layers will not "notice" the non-uniformity.

Laser ablation is a fast and versatile tool to fabricate these features. The size of the cavity should be slightly larger than the size of the chips, meaning that this can be several square millimeters and though we still want good nice vertical cavity sidewalls and high dimensional accuracy. The Excimer laser has the right specifications for this purpose, large areas can be ablated with still very good shape and dimensional control ability.

The copper heat sink at the bottom of the cavity acts as a perfect laserstop for the Excimer laser light (248 nm wavelength). The polymer on top of the heat sink will be ablated, while the copper will reflect the light and stays intact. This way, it is possible to remove all the polymer on top of the heat sink, resulting in a perfectly flat bottom of the cavity. For fast processing, we chose to perform dynamic laser

Table 6.6: Optimized process flow for the realization of a 28 μm thick SU-8 10 layer on top of a 17 μm thick copper island

SU8-10 28μm optimized process flow	
Process step	Process parameters
Room temperature conditioning	Out of fridge 60 min. before process
Deposit SU-8 10	poor from bottle
Remove visible air bubbles	small pipette
Spin-coat	1250 rpm
Pre-bake 1	3 min. @ 65 ^{o}C
Pre-bake 2	7 min. @ 95 ^{o}C
UV-exposure	60 s / 10 mW/cm^2
Post exposure bake 1	1 min. @ 65 ^{o}C
Post exposure bake 2	3 min. @ 95 ^{o}C
Deposit SU-8 10	poor from bottle
Remove visible air bubbles	small pipette
Spin-coat	1500 rpm
Pre-bake 1	3 min. @ 65 ^{o}C
Pre-bake 2	7 min. @ 95 ^{o}C
UV-exposure	60 s / 10 mW/cm^2
Post exposure bake 1	1 min. @ 65 ^{o}C
Post exposure bake 2	3 min. @ 95 ^{o}C
Hard bake	60 min. @ 150 ^{o}C

ablation in which the sample is moved around by a high precision XY translation stage (accuracy = 1 μm), while the laser is pulsing continuously. This way, the complete cavity area will be scanned. The laser parameters are summed up in Table 6.7.

Table 6.7: Dynamic laser ablation parameters for the realization of a cavity inside SU-8 material.

SU-8 cavity laser ablation parameters	
Laser power	6 mJ
Attenuation	0 degrees
Pulse repetition frequency	200 Hz
Fluence	138 mJ/cm^2
Stage translation speed	200 μm /s
Projection mask dimensions	3000 x 3000 μm ^{2} square

When using Truemode™ Backplane Polymer as embedding material, the same parameters can be used. The size of the cavity is chosen in such a way that the gap between the embedded chip and the cavity edge is about 25 μm . When the

embedding polymer layer is about 25 μm thick, the aspect ratio of the gap would be 1:1 which is ideal concerning planarity. If the aspect ratio would be too high (narrow gap), the change of air bubble insertion would become a problem, while a low aspect ratio (wide gap) would result in poor planarization of the next layer. This is shown schematically in Figure 6.2.

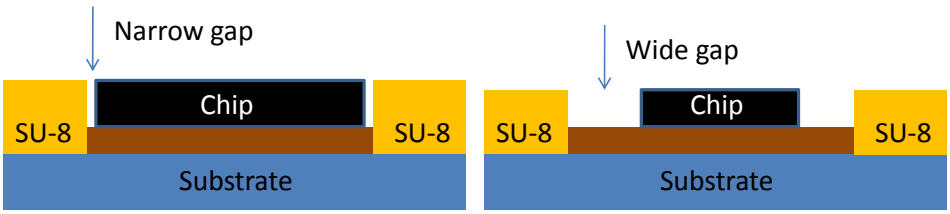


Figure 6.2: Schematic view on the aspect ratio of the gap between the embedded die and the cavity edge.

Inherent to dynamic laser ablation is the linear depth profile at the beginning and end point of a dynamic laser ablated area. This results in the fact that there will still be unremoved SU-8 material in the corners of the cavity. This residual material is then removed by applying static ablation in the four corners. 300 pulses with the same laser parameters as the scanning parameters shown in Table 6.7 are sufficient.
Because a lot of material is actually removed, a third and final ablated step is necessary to remove the debris. In this step, the cavity area is again scanned with the same laser parameters, but with a much higher speed of 1000 μm /s.

The resulting substrate progression at this stage is shown schematically in Fig. 6.1 (h).

6.2.4 Placing of the chip

The placement of the chips during the PhD research period was performed manually. During this time a fine-pitch pick and place tool from Dr. Treski was installed in the cleanroom, however it was only fully functional at the end of this period. So no investigation was done to define the feasibilities of this tool. The specifications of the tool given by the providers are promising though. An alignment accuracy less than 3 μm could be achieved, mainly determined by the visual system as is often the case with this kind of machinery. A dedicated chuck can pick up very small die sizes of 120 μm , and does not harm 20 μm thin chips as was tested already on the set-up. The machine also has a feature to heat the chip locally to 350 ^{o}C. Figure 6.3 shows a picture.

The requirements for the chip placement accuracy depends on the final application. In Section 6.3, we describe the fabrication process of waveguides on top of embededd opto-electronics and the accuracy of the waveguide positioning with respect to the opto-electronics underneath. The waveguide fabrication process defines thus the alignment accuracy. In case there is only one emitter array and one receiver array, the placement of the chips can be done coarsely. When however multiple emitter and reveiver chips must be placed, they should be well aligned with respect to each other. Figure 7.3 in Section 7.2 shows the optical losses due to misalignment of the chip with respect to the waveguides. The 0.5 dB point is around 8 μm. This means that the alignment accuracy of the chips should be a few μm.

The manual placing of the very thin (20 μm) and small dies (1000 x 350 μm^2) is a matter of careful handling. The success and yield of the placing process depends on the experience of the operator. However with the right tools and the right methods, anyone can learn this procedure quite fast. Once the operator has a hang of it, the chip placing yield is close to 100%.

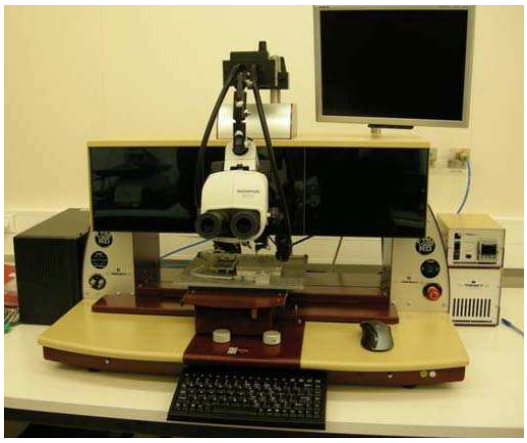


Figure 6.3: Dr. Treski fine-pitch placer installed in the cleanrooms of CMST Microsystems.

Fixing of the chip inside the cavity is done with dedicated glue. For this purpose, we chose a high fluidic flip-chip underfill material U 8449-9 from Namics Corporation [3]. It is a capillary flow type material which penetrates between the chip and the substrate. It is claimed to show very good fluidity, high reliability and high temperature conductivity. The U8449-9 is not commercially available, but the commercially available U8443 series are supposed to have the same characteristics, which are shown in Table 6.8. Curing of the glue is done thermally on 150 ^{o}C for 5 minutes.

Table 6.8: Providers specifications of the U8443 underfill material of Namics Corporation Japan.

U8443 Underfill material specifications	
Viscosity (Pa.s)	8.0
Glass Transition Temperature (^{o}C)	125
Modulus (Gpa)	6.5
α1 (ppm)	38
α2 (ppm)	125

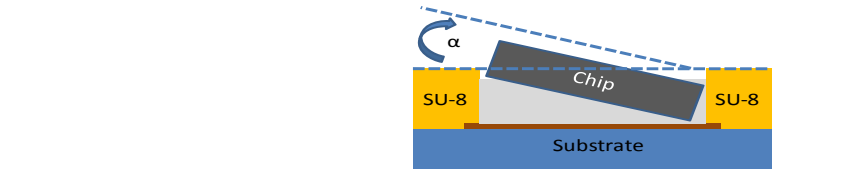
Dispensing the right amount of glue is decisive for the success of the chip placement. When dispensing too much, the glue will flow over the chip surface after leveling. The glue should not be covering the active light emitting- or detecting areas since it is not transparent. The glue should also not cover the contact pads of the chip since the glue cannot be laser ablated with the Excimer, Nd:YAG or CO_2 lasers at CMST after curing without harming the contact pads. Too little glue will result in an air gap between the chip and the heat sink, which will have a detrimental effect on the reliability of the system because air tends to expand a lot more than its surrounding material when heated. When a large syringe is used, the drops will be too large, while fine syringes cannot be used since the material cannot be pressed through the needle. A good technique is dipping the tip of a fine syringe in a bubble of glue so that a small amount of glue is sticking to the needle tip. Touching the cavity bottom with the glue covered needle results in a capillary spreading of the glue over the cavity bottom. For large scale production, this technique should be automated.

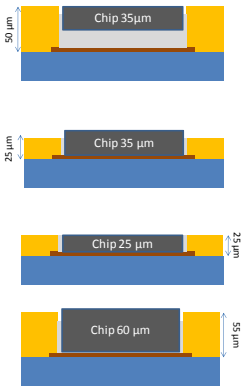
After the thinning of the chips (see Chapter 5), they are not released from their temporary glass carrier but are kept in that state until the chips need to be placed. At that stage they are still mounted in wax. When putting the complete glass carrier in an acetone bath, the wax will dissolve and the chips are released. When releasing, the chips however start to float in the acetone and can end up in the bottom of the acetone bath where they are difficult to be grabbed. At any moment of the chip placement procedure, one must prevent to use tweezers, since it will damage or break the fragile GaAs chips. A much better approach is the dispensing of little acetone on the glass carrier, so the chip can release, but will not flow away. Once it is not attached to the glass carrier anymore, the chip should be transferred to a soft tissue where it can be cleaned. This transfer is done by tilting the glass carrier and flush the chip down on to the tissue with an acetone flow. Once on the tissue, a few drops of acetone on the chip are sufficient to clean it from any residues of wax material. The chip can be transferred directly from the soft tissue onto the substrate simply by holding the tissue above the substrate and tilt it. When the chip is lying on the substrate, it must be pushed inside the

cavity. This is best done with a soft pushing device like a piece of paper or a paper filter. When the chip is lying upside down, it can be flipped with the same pushing device. The chips need to be in the right XY position in the middle of the cavity, which is easily feasible by pushing the chip to the middle of the cavity when looking through the microscope. The Z position of the chip is fixed in a next leveling step. The chips position at this stage is shown schematically in Fig. 6.1 (i).

As mentioned above, the cavity embedding approach was chosen for planarization purposes. To achieve planarization however, the chip must be mounted in the cavity in such a way that it is completely parallel with the top surface of the embedding surrounding layer. Therefore we apply an additional leveling step which consists of the pressing of the chip inside the cavity with a leveler as is clarified in 6.1 (j). The leveler can be anything with a flat surface.
The degree of leveling can be seen as a quantification of how parallel the chip surface is with respect to the embedding layer surface plane. A good value for this quantification is the tilt angle of the chip surface with the embedding layer surface plane as the reference plane. This is shown clearly in Figure 6.4 (top). The defining parameter for the leveling is the cavity depth versus the chip thickness. Figure 6.4 (bottom) compares the chip tilt angles for different cavity depths and chip thicknesses. The chip tilt angle is measured along the width of the chips, since the tilt angle over the length axis is always much smaller due to the longer distance. We make a difference between VCSEL's (350 μm width) and Photodetectors (450 μm width) since they have a different width. Logically, larger dies will be leveled better than smaller ones as can be seen in the values in Figure 6.4, where the tilt angles for the Photodiodes are always a bit smaller than those for the VCSEL's.

The measurements show that the best leveling is obtained when the chip thickness is equal or larger than the cavity depth. All the measured tilt angles are below 1 degree, which is an acceptable value. The additional losses due to the chip tilt angle are simulated and discussed in Chapter 7, Section 7.2. When the cavity is deeper than the thickness of the chip, the latter has a higher degree of movement ability resulting in a higher average tilt angle. As a consequence, we must have good control over the cavity depth and/or the chip thickness. The cavity depth is dependent on the embedding layer thickness and can vary over multiple micrometers (see Figure 6.5). For good leveling we measure the cavity depths after laser ablation and adjust the chip thickness by controlling the polishing time. The thickness of the glue is about 3 μm if the chip is firmly pushed down with the leveler. This 3 μm thickness is taken into account when adjusting the chip thickness.





	VCSEL	Photodiode
Population (pcs)	4	4
Average α (degrees)	1.2	1.1
Standard deviation α (degrees)	0.4	0.6

	VCSEL	Photodiode
Population (pcs)	3	4
Average α (degrees)	0.6	0.5
Standard deviation α (degrees)	0.3	0.2

	VCSEL	Photodiode
Population (pcs)	9	8
Average α (degrees)	0.2	0.1
Standard deviation α (degrees)	0.3	0.3

	VCSEL	Photodiode
Population (pcs)	8	7
Average α (degrees)	0.4	0.3
Standard deviation α (degrees)	0.3	0.3

Figure 6.4: Tilt angle of a placed and leveled chip inside a laser ablated cavity with respect to the embedding layer surface plane.

6.2.5 SU-8 covering layer

When the underfill glue is cured, the chip is firmly fixed inside the cavity. Another spin coated SU-8 layer will cover the chip and physically complete the embedding (see Fig. 6.1(k)). The process flow for this covering layer is the same as shown in Table 6.6, but only one layer is spincoated and with a spinspeed of 2000 rpm, resulting in a layer of 5 to 15 μm on top of the chip. This variation in thickness is the sum of a variation in cover layer thickness, embedding layer thickness, chip thickness and chip tilt angle.
The SU-8 acts as a very good covering material. No bubble insertion in the gap around the chip was ever observed. The SU-8 does not show any sign of delamination on top of the chip and shows good planarization. Figure 6.5 shows cross-sections of a fully embedded 45 μm thin VCSEL with a close up on the gap between the VCSEL and the cavity edge. For a narrow gap with an aspect ratio lower than 1:1 (Figure 6.5 bottom right), the planarization is almost perfect and no air bubble insertion is seen despite the high aspect ratio. For the wider gap (Figure 6.5 bottom left), a soft dip of a few μm can be seen at the covering layer surface.

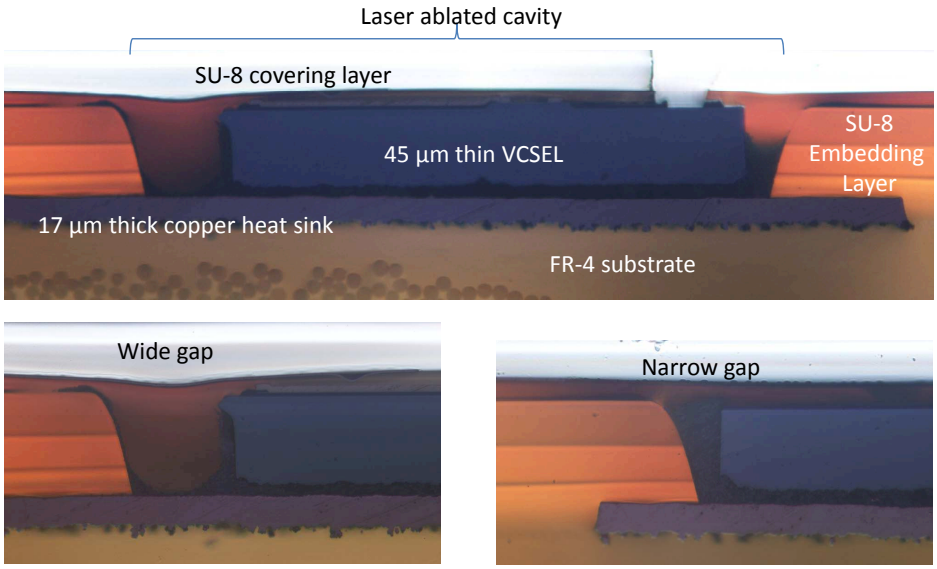


Figure 6.5: Cross-sectional photograph of a fully embedded 45 μm thin VCSEL inside SU-8 material and a close-up on the filling of the VCSEL-cavity gap for a narrow and a wider gap.

6.3 Waveguide fabrication on top of embedded dies

The opto-electronic devices are now successfully embedded inside an SU-8 layer build-up. The waveguide stack is then fabricated on top. The fabrication and characterization of these waveguides is firmly described in Chapter 3. In this section, we only focus on the alignment of waveguides with respect to the embedded opto-electronics. The alignment is performed actively on a standard PCB photo-lithography aligner tool at CMST (SET MG1410). Since the optical waveguide materials act as a negative photoresist, the used photolithography mask is negative, meaning that the only openings of the mask are the waveguide features. Through the visual microscope system of the aligner, we can look through these openings and see the opto-electronic components. The alignment must be done with respect to the active areas of the VCSELs as well as the photodiodes, which are clearly visible. This approach can be used for aligning a single waveguide array. If multiple waveguide arrays need to be applied, we have to make sure that all the embedded components are positioned within a $\pm$ 5 μm positioning tolerance. The opto-electronic components are however placed manually inside the cavity, resulting in a $\pm$ 25 μm alignment error which is too high. The placement of the chips with a fine pitch placer, as depicted in Section 6.2.4 can enable

a much higher accuracy, which allows us to align any waveguide routing scheme with respect to the embedded chips. Table 6.9 shows the average alignment error, the standard deviation and the maximum deviation of the waveguides measured for 7 samples.

Table 6.9: Aligment error measurements of waveguides with respect to the underlying embedded opto-electronics.

Alignment error of waveguides with respect to embedded chip		
	VCSEL	Photodiode
Population	7	7
Average alignment error (μm)	4.9	5.7
Standard deviation (μm)	2.2	3.1
Maximum deviation	7.8	9.2

The alignment error is within a 10 μm tolerance which is satisfactory (see the simulations in Chapter 7 Section 7.2). Figure 6.6 shows microscope pictures of finished waveguides on top of an embedded VCSEL (top) and a photodiode (bottom).

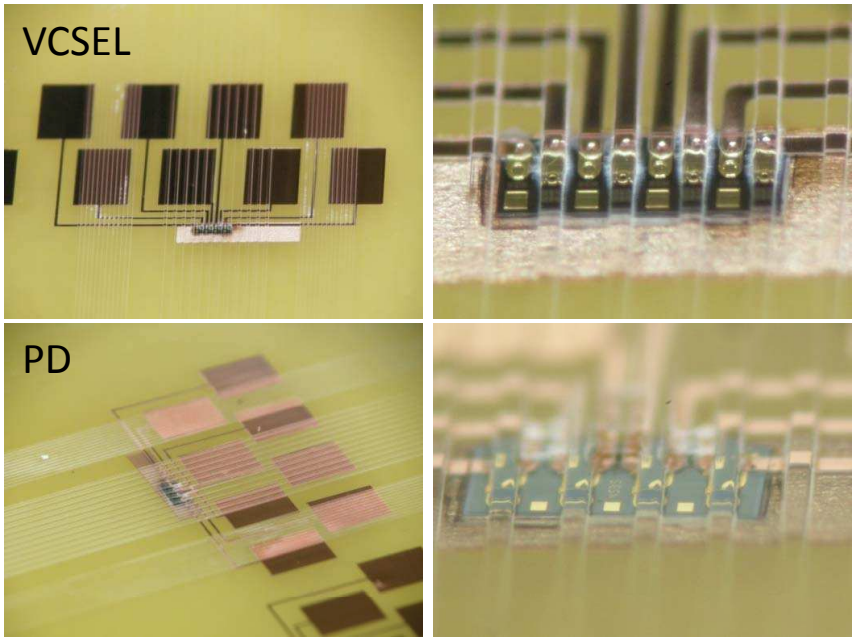


Figure 6.6: Microscope pictures of finished waveguides on top of an embedded VCSEL (top) and a photodiode (bottom).

6.4 Galvanic interconnection of embedded chips

6.4.1 Laser ablated micro-via's

All the electronics and opto-electronics which need to be thinned down, need to have only top contacts. Since the substrate of the chip is lapped and polished, any contact at the back side would disappear. Because of only the presence of top side contacts, it is possible to contact an embedded chip completely from above using micro-via's through the upperlying polymer layers. Laser ablation is a widely used fabrication method for the realization of through-via's and blind via's. At CMST Microsystems, an Nd:YAG laser (355 nm), a CO_2 laser (9.6 μm) and a KrF Excimer (248 nm) laser are available.
The Nd:YAG laser has a Gaussian profile which makes it hard to use as via ablating tool. The energy in the middle of the beam is much higher than at the edge of the beam. This results in the damaging of the contact pads in the middle of the beam, while the polymer at the outside of the beam still needs to be ablated. Quick tests with varying laser parameters did not deliver any good results. Three lenses are installed on the laser to shape the beam from a Gaussian to a flat-top beam, but all efforts to achieve a satisfactory uniform beam were unsuccessful. Therefore we will focus on the Excimer and CO_2 laser in what follows.

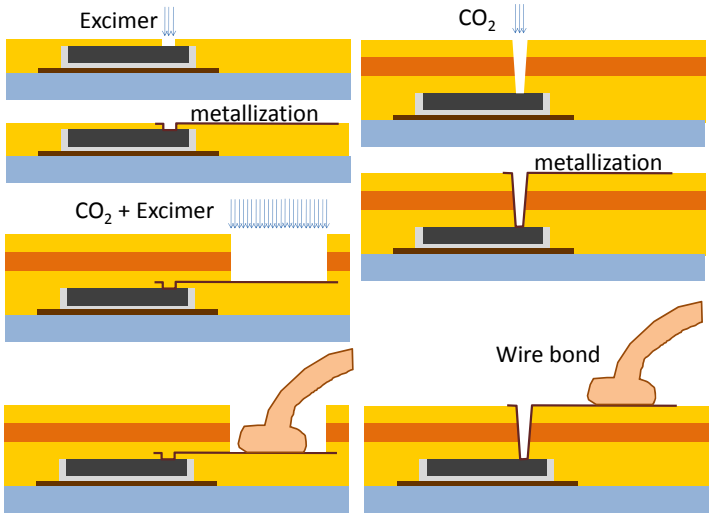


Figure 6.7: Schematic process flow for the fabrication of metalized micro-via's to the contact pads of embedded dies.

The choice of laser strongly depends on the choice of via approach. Figure 6.7 shows the schematic process flow for 2 main approaches for the fabrication of

metalized micro-via's to the contact pads of embedded dies. The approach in Figure 6.7 (left) consists of the laser ablation of via's right after the chip embedding process. This way, the via's are ablated in an SU-8 layer of 5 μm to 15 μm thickness. For such a low aspect ratio via's, the Excimer laser showed the best results. The visual camera system for the Excimer laser has a higher magnification than the CO_2 laser, simplifying the alignment process. Because the optical waveguide layers are processed on top, the metallization layers will be embedded inside the build-up as is clearly explained in the schematic process flow, Figure 6.7. An additional contact pad opening step is however needed. Figure 6.8 shows pictures of Excimer laser ablated via's to an embedded photodiode (a), after metallization of the via's (b) and the metallization etching for an embedded VCSEL (c). Close-ups of these via's are shown in respectively Figure 6.8 (d), (e) and (f) respectively. The parameters of the Excimer laser via ablation parameters can be found in Table 6.10.

Table 6.10: Excimer and CO_2 laser ablation parameters for the fabrication of micro-via's to embedded opto-electronic components in SU-8.

CO_2 laser via-ablation parameters	
Laser parameter	Parameter value
Energy level	1
Attenuation	0 degrees
Lens	L1
Projection mask	500 μm diameter circular
# pulses	20
Puls repetition frequency	100 Hz
Fluence	21.7 J/cm^2
Excimer laser via-ablation parameters	
Laser parameter	Parameter value
Puls Energy	3 mJ
Projection mask	400 μm diameter circular
# pulses	50
Puls repetition frequency	140
Fluence	58 mJ/cm^2

A second via approach (Figure 6.7 (right)) consists of the laser ablation of the via's after the fabrication of the waveguide layers. The pitch of the contact pads of the embedded chips is 125 μm and the size of the contact pads are 80 x 80 μm ^{2} for a VCSEL array and 60 x 70 μm ^{2} for a PD array. Taking the alignment tolerance into account, the via's need to have a maximum diameter of 45 μm at the bottom. The waveguide layers however have a total thickness of 120-150 μm. This means that the aspect ratio of the via's can be up to 3:1. The Excimer laser did not succeed to fabricate such a small, high aspect ratio via's without damag-

ing the contact pads. The main reason for this, is the high tapering angle of the SU-8 material when using an Excimer laser. When using the CO_2 laser, the via's were ablated successful, but the alignment becomes crucial. The visual system of the CO_2 laser has a lower magnification and the camera viewing axis is different from the laser beam axis. This latter forces us to compensate the angle between both axes during alignment. Good alignment can be achieved, but is more time-consuming than with the Excimer laser via approach explained above. Figure 6.9 shows photographs of CO_2 laser ablated via's to an embedded photodiode (a), after metallization of the via's (b) and the metallization etching for an embedded VCSEL (c). Close-ups of these via's are shown in Figure 6.9 (d), (e) and (f) respectively. The parameters of the CO_2 laser via ablation parameters can be found in Table 6.10.

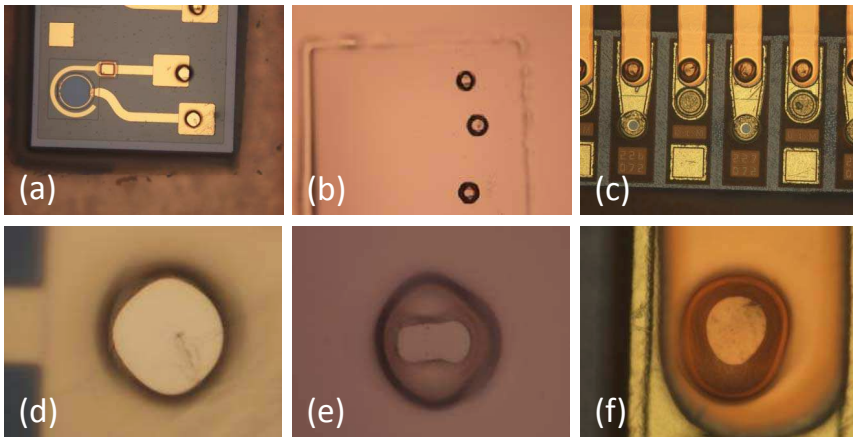


Figure 6.8: Pictures of Excimer laser ablated via's to embedded opto-electronic components

The metallization of high aspect ratio CO_2 laser ablated via's using a sputter process (detail: see Section 6.4.2) exposes a critical problem: the metallization of the via side walls at the bottom of the via is not complete. This means there will be no contact to the embedded chip. Figure 6.10 shows a cross-section and close-ups to show the lack of copper at the bottom via side walls. The side walls show a ridged profile, which seems to be inherent to the CO_2 laser ablation of SU-8. This profile causes no problem at the top half of the via, but at the bottom this becomes a prominent problem, cause the sputtered Cu particles cannot reach the total side wall surface. Figure 6.10 also shows a SEM picture inside the via, revealing the ridges clearly.

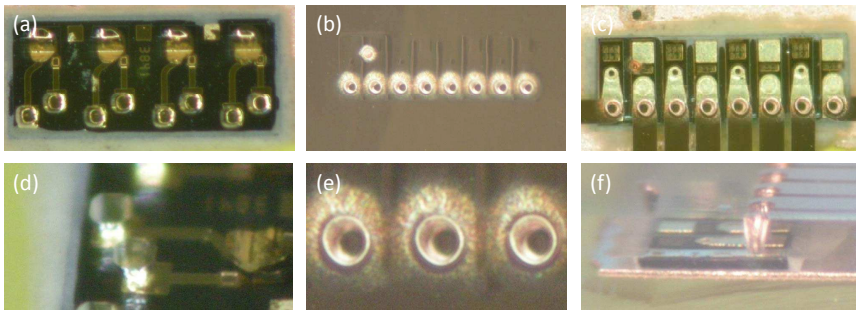


Figure 6.9: Photographs of CO_2 laser ablated via's to embedded opto-electronic components

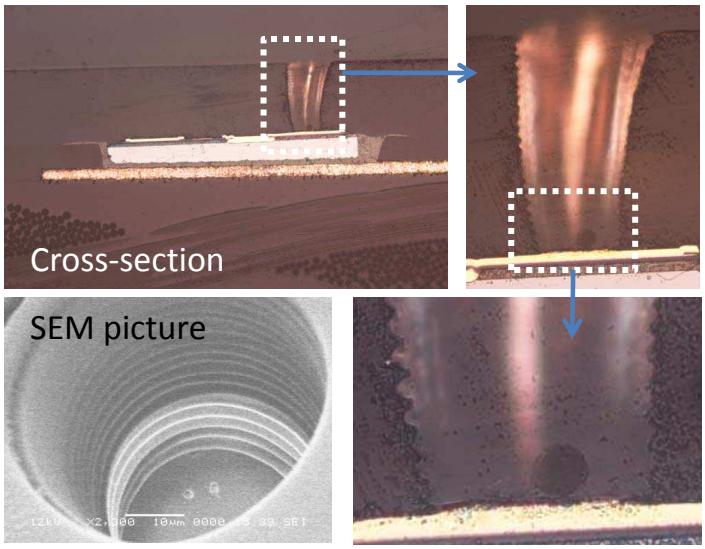


Figure 6.10: Cross-section of a CO_2 laser ablated via through the waveguide layers to the contact pad of an embedded VCSEL and an SEM picture thereof.

6.4.2 Metallization

The metallization of the via's and the fan-out to larger contact is done using a sputter process. The same sputter process as for the seed layer of the heat sink (see Section 6.2.1) was used, with the same process parameters (see Table 6.3). After sputtering a 50 nm TiW and a 1 μm copper layer consecutively, both layers are etched into the final lay-out. First a photoresist layer AZ 4562 is applied (parameters: Table 6.1). Then the copper layer is etched in a Iron(III)-chloride

solution (also called ferric chloride). This etchant etches much slower (0.25 μm /minute) than the one used for the heat sink copper layer ($CuCl_2$ / Hcl solution - 6 μm /minute), resulting in a better etch resolution. The TiW is then etched in a hydrogen peroxide bath. The photoresist which is then still on the fan-out is removed in a stripping process consisting of a consecutively 2 minutes Acetone bath strip, a 2 minutes Acetone/IPA bath strip and an IPA rinse. Figure 6.11 shows photographs of the different steps of the process flow.

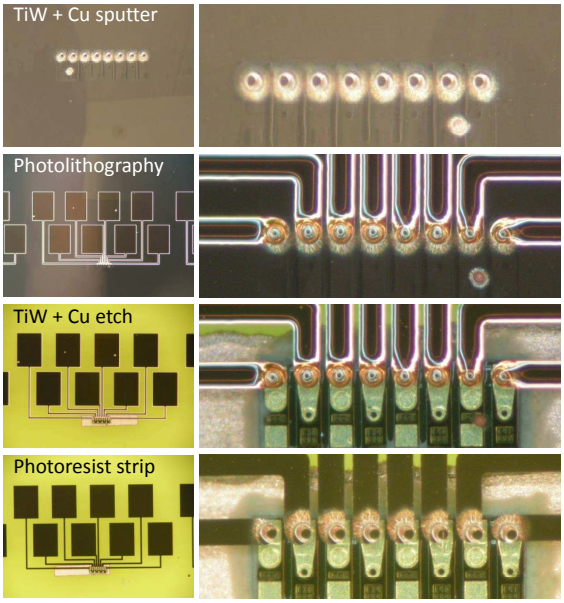


Figure 6.11: Process flow for the metallization of CO_2 laser ablated via's and fan-out from and to embedded opto-electronics in SU-8.

The fan-out track resolution which can be obtained with the use of above mentioned photoresist and etchants has been investigated with a dedicated resolution test mask. The results are shown in Figure 6.12 which shows pictures of tracks for varying track width and track pitch. A track pitch of 20 μm and a track width down to 7.5 μm is perfectly achievable (see Figure 6.12 bottom right).

The sputtering of Cu on top of a cured Truemode™ Backplane Polymer layer revealed that the proposed baking temperature of the Truemode™ Backplane Polymer, which was noted in the material process datasheets from the providers, was not correct. Figure 6.13 left shows pictures of Cu sputtered Truemode™ Backplane Polymer layers which had undergone a hardbake of 120^{o}C, 150^{o}Cand 210^{o}C. The 2 samples on the left were hardbaked for 30 minutes (top left) and 5 hours (bottom left) on 120^{o}C. They look very pale compared to those baked at

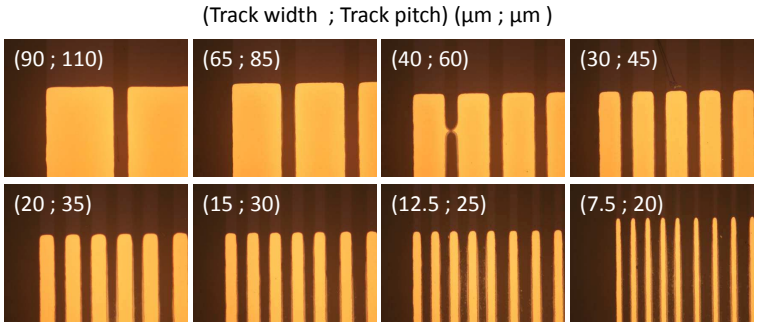


Figure 6.12: Copper fan-out etching resolution test

150^{o}C and 210^{o}C. The 100 times magnified microscopic view on the surface (Figure 6.13 right) shows that the surface is wrinkled on the micron-scale. The 100X magnified picture of the 150^{o}C sample shows a strange looking track, which is actually a line of a ballpoint which was deliberate made to be able to focus on the surface level. From these pictures, we can conclude that the 120^{o}C hardbake temperature is too low for the Truemode™ Backplane Polymer material and should be at least 150 ^{o}C.

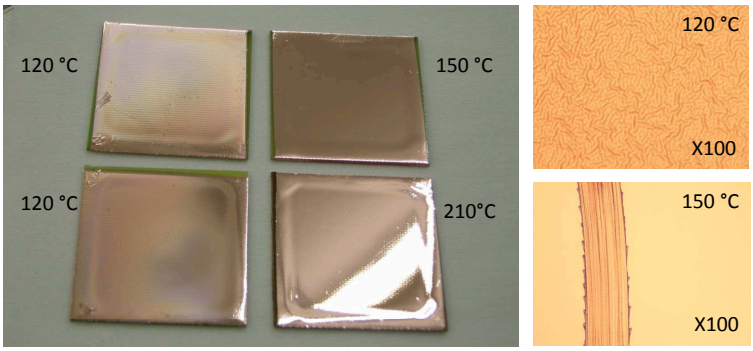


Figure 6.13: Pictures of 1 μm thick sputtered Cu on a Truemode™ Backplane Polymer layer which was cured at 120^{o}C, 150^{o}C and 210^{o}C.

The adhesion of the metal layer to the polymer layers and vice versa can become a restrictive reliability issue. It is hard to determine "how good" they have to adhere to each other. Reliability testing should answer this question. A few tests however allow us to quantify the adhesion strength. One of them is the peel strength test. This consists of the fabrication of strips of metal on top of the polymer and measure the force needed to pull the strip from the polymer substrate. These measurements were done for (1μm Cu)-strips and (50 nm TiW + 1 μm Cu)-

strips of 3 mm width on top of a PI2525, SU-8 and Truemode™ Backplane Polymer layer. To be able to pull the metal strips without breaking them, they are electroplated to a final thickness of about 20 μm. The results are shown in Figure 6.14. The metal adheres very well to PI2525, while poor to SU-8 and Truemode™ Backplane Polymer. The use of an intermediate 50 nm thick TiW layer proves its usefulness as an adhesive layer, since it almost doubles the peel strength. The peel strength shown in the Figure 6.14 is expressed in units of weight (g), while as often the unit N/m is used. If X is the value expressed in "g" and Y the value expressed in "N/m", then is Y = (10*(X*10E-3))/3E-3 (3E-3 stands for the 3 mm width of the strip).

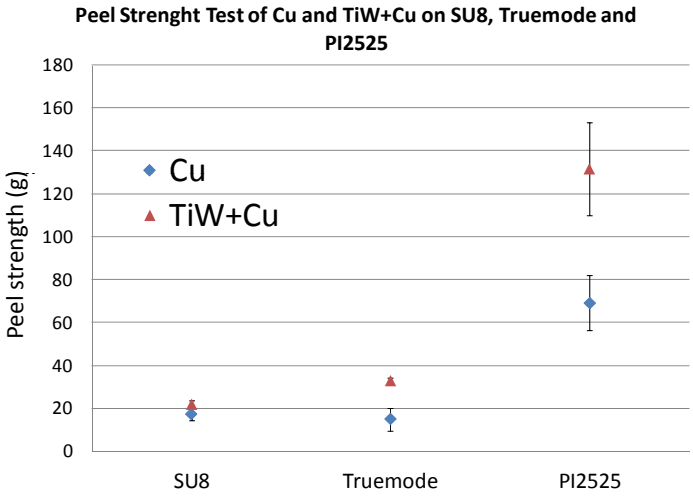


Figure 6.14: Peel strength test results of (1μm Cu)-strips and (50 nm TiW + 1 μm Cu)-strips on top of a PI2525, SU-8 and Truemode™ Backplane Polymer layer.

Figure 6.15 shows pictures of pulled (1μm Cu)-strips (Fig. 6.15(b)) and (50 nm TiW + 1 μm Cu)-strips (Fig. 6.15(c)). The first photograph (Fig. 6.15(a)) shows the pulling of the Cu strip from the TiW strip. Normally the adhesion between the Cu and the TiW should be very good and they should not be able to be separated like shown on the picture. The reason for this unusual behavior was found in the sputter target. Copper targets which have not been used for a while and which have been exposed to environmental humidity can contain residual contaminants adsorbed or absorbed on the surface of the target which may adversely affect the quality of the sputtered film and reduce particle levels to unacceptable limits. Therefore the target must be conditioned or burned-in before it can be used again, which was not the case for the substrate in Fig. 6.15(a)).

Since the metal tracks will be embedded in between polymer layers, it is also important that the polymer adheres well to the copper. Since Truemode™

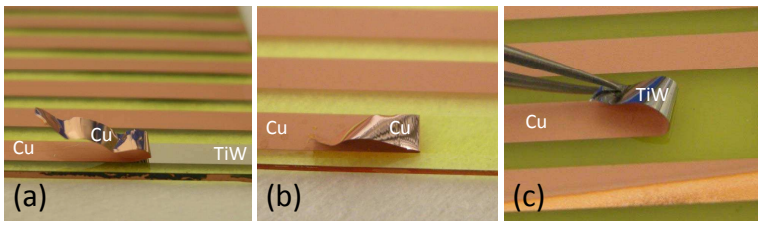


Figure 6.15: Pulling of the 3 mm wide metal strips for the peel strength tests.

Backplane Polymer is very brittle, it cannot be peeled off from the metal without breaking, eliminating the possibility of using peel strength tests. Standard smaller tests are the Scotch tape test and the scratch test. The Scotch tape test consists of the mounting of Scotch tape on top of the Truemode™ Backplane Polymer layer and pull it off abruptly. The Truemode™ Backplane Polymer was not damaged and still adheres to the sputtered copper layer (Figure6.16(a)). The scratch test consists of the scratching of the Truemode™ Backplane Polymer layer and looking around the scratch whether the Truemode™ Backplane Polymer disadheres from the sputtered copper or not. Figure 6.16(b) and (c) shows the results. There is a clearly visible area around the scratch, where the Truemode™ Backplane Polymer disadheres. This means that the stress inside the Truemode™ Backplane Polymer material layer, caused by the scratching, was higher than the adhesion strength between the Truemode™ Backplane Polymer and the sputtered copper. This means that the adhesion is not very strong.

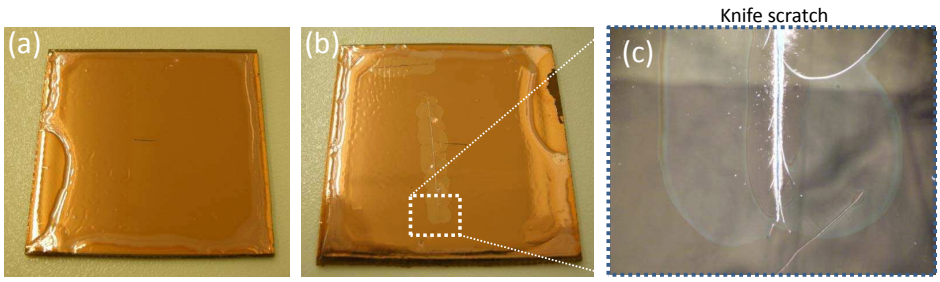


Figure 6.16: Scotch tape test (a) and scratch test (b)&(c) of a 30 μm thick copper layer on top of a 1 μm thin sputtered layer

The final embedded copper tracks are 1 μm thick which is thick enough by means of contacting the embedded dies. With respect to reliability of the system, it is preferable to plate the metal tracks to obtain much thicker tracks (typical about 15 μm thick). Three different approaches has been investigated at CMST in the framework of another PhD research [4]. Figure 6.17 shows the 3 approaches

schematically.

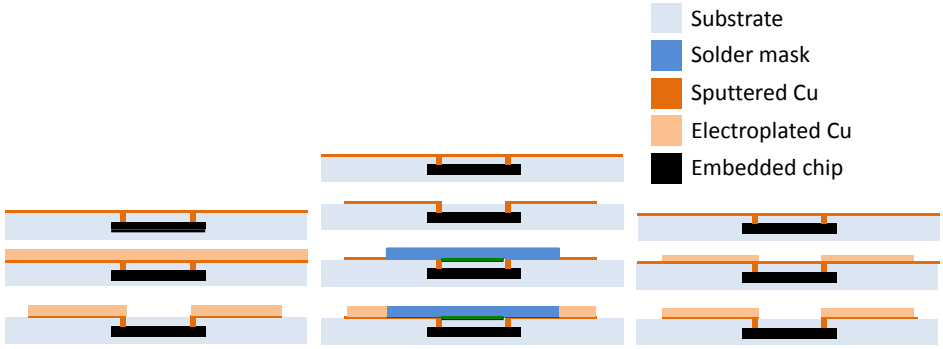


Figure 6.17: Three approaches for the plating of the fan-out of the galvanic interconnections towards embedded dies

A first possible approach (Fig. 6.17(left)) is the plating of the complete sputtered Cu layer, followed by the etching of the obtained thick Cu layer. Etching of a thick Cu layer has a limiting effect on the smallest feasible track pitch, since underetching starts to occur. A second approach (Fig. 6.17(center)) consists of etching the thin sputtered Cu, covering it with solder mask (except on the large contact pads) and then plate only the contact pads. This improves the reliability of the contact pads, but the embedded tracks are still very thin. The third approach showed to be the best and consists of a pattern plating step. On top of the sputtered copper, a photoresist layer is applied everywhere except on the places where the tracks are supposed to be. Then the sample is plated, resulting in a selective plated substrate with only thick copper on the places without photoresist. Finally the photoresist is removed and the copper is etched shortly to remove the sputtered Cu layer and leave the thick copper. Using this method, small pitches are still feasible and the complete via's and fan-out consists of thick copper.
These technologies were not included in this PhD work to reduce the processing time of the substrates. Plating can be a quite time consuming process and the thick copper layer is only useful when it comes to reliability.

6.4.3 Truemode™ Backplane Polymer galvanic via interruption

In Chapter 4, the Truemode™ Backplane Polymer as waveguide material showed its good bending properties, low optical bending loss and good processability. The embedding of actives inside the Truemode™ Backplane Polymer however causes a major problem, which will be explained in this section. It is for this reason that all the components embedding described in this work is done in SU-8

material.

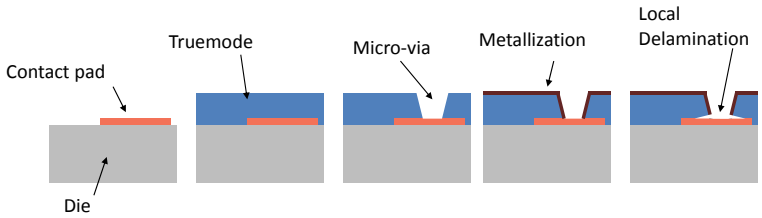


Figure 6.18: Schematic overview of the contact delamination problem during the embedding of actives inside Truemode™ Backplane Polymer material.

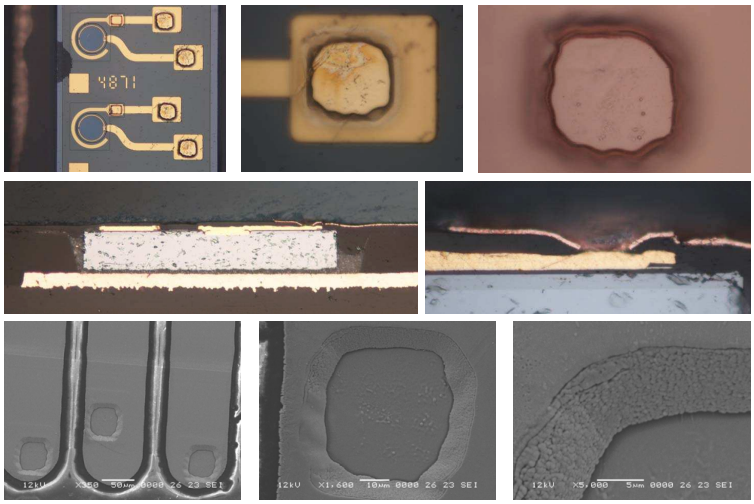


Figure 6.19: Microscopic pictures (top), cross-sections (center) and SEM pictures (bottom) of the contact pad delamination of Truemode™ Backplane Polymer .

The problem takes place during the laser ablation or metallization of the micro-via's. The Truemode™ Backplane Polymer layer seems to be delaminating locally from the contact pads of the embedded chip, causing an interruption in the galvanic interconnection. The delamination problem is visible after the metallization of the via. Figure 6.18 shows a schematic explanation and Figure 6.19 shows microscopic pictures (top), a cross-section (center) and SEM pictures (bottom) of the delamination. Three different possible solutions for this problem were examined and are described in what follows. Figure 6.20 shows a cross-section of an Excimer laser ablated via through SU-8, showing no delamination at all, as it should be.

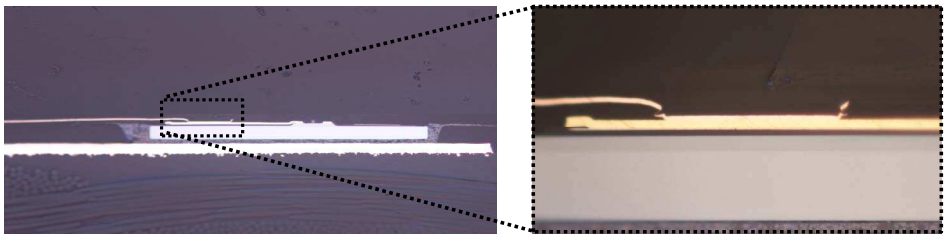


Figure 6.20: Cross-section of an Excimer laser ablated via through the SU-8 chip covering layer

Chemical treatment of the contact pad

The contact pads of the embedded actives are coated with a Au film. In an effort to improve the adhesion between the Truemode™ Backplane Polymer and the Au finish, we tried to chemically treat the gold. Collaboration with the Polymer Chemistry and Biomaterials Group (PBM Group) of the Ghent University is ongoing. The use of thiols was proposed since their proven effect on gold and the possibility to attach active acrylate groups onto the gold (Truemode™ Backplane Polymer is a methacrylate). First tests were done to determine the hydrofilicity of gold after treatment with different kinds of thiols. Table 6.11 shows the contact angle measurements of a drop of water on top of a gold finished substrate. Further research is ongoing to determine which contact angle would be the most preferable. However, we are not sure that the enhancement of the adhesion between gold and Truemode™ Backplane Polymer will solve the problem. Other factors like local stress could also be the reason for the delamination.

Table 6.11: Contact angle of water on Gold finished substrates, impregnated with different thioles

Water contact angles on thiol impregnated Au					
	1-butane thiol	Allyl mercaptane	2-amino ethanethiol hydrochloride	dodecane thiol	Reference
Avg. CA	64	51	41	85	63
Stdev. CA	5.6	3.4	5.8	3.6	2.4

Metal paste via filling

A second approach is the filling of the via's with conductive metal paste. Figure 6.21 shows pictures of the dispensing and scraping of the paste. The paste is dispensed using a syringe tip, comparable to the dispensing method of the underfill

glue in Section 6.2.4. The scraping is done manually using a cleanroom tissue for the proof-of-concept, but stencil printing would be a more appropriate way for reproducible results. This approach has proven to fix the galvanic contact, but is not preferable. The contact delamination is still present, resulting in an air gap between the Truemode™ Backplane Polymer layer and the contact pad, which is not favorable.

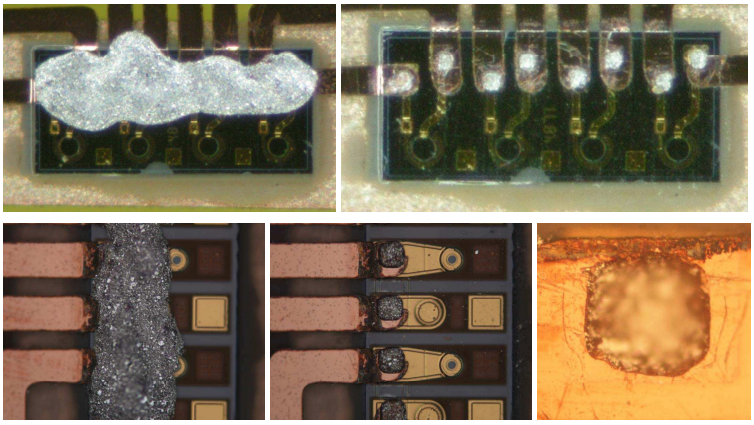


Figure 6.21: Metal paste via filling pictures.

Polyimide adhesion layer

In Chapter 4, Section 4.6, PI2525 Polyimide proved to adhere very good to Truemode™ Backplane Polymer. The chip surface is also covered with a passifying and protective Polyimide layer but with other properties than the PI2525 Polyimide. We can expect that PI2525 could be a possible intermediate adhesion layer between the chip with protective Polyimide layer and the Truemode™ Backplane Polymer. This principle has been investigated, pointing out that there is still an adhesion problem at the location of the chip, possibly caused by bad adhesion between the chip covering Polyimide and the PI2525. Figure 6.22 shows the local delamination around the laser ablated micro-via's (left). The right picture shows via's which did not delaminate, and showed good galvanic contact later on in the process, but this process shows bad reproducibility.

6.4.4 Contact opening

In Section 6.7, two different approaches for the via-contacting of embedded dies were proposed, while only one proved to be feasible: the approach with the low

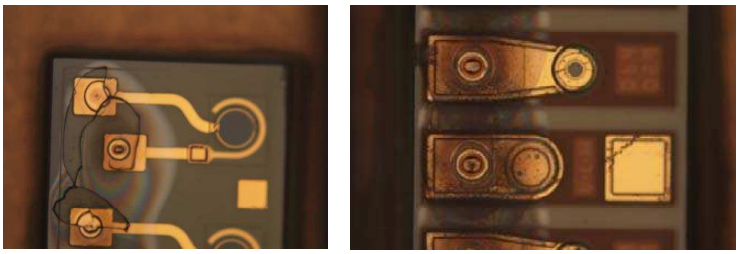


Figure 6.22: Pictures showing the local delamination around the laser ablated micro-via's, using PI2525 as an intermediate adhesion layer.

aspect ratio via's and embedded copper tracks. The metallization tracks are covered with the waveguide stack layers which are applied later on in the process. To contact these embedded copper tracks, they must be opened by removing all polymer on top of it. The polymer/metal laser ablation selectivity of the CO_2 laser allows us to remove all polymer material above the metal tracks, which acts as a laser stop. The optimized CO_2 laser parameters are shown in Table 6.13. Because the laser beam size is much smaller than the contact opening size, a scanning technique is used, performing the same laser process over and over again while moving the sample. A cross section of an opened contact pad is shown in Figure6.23.

Table 6.12: CO_2 laser ablation parameters for the opening of large embedded contact pads.

CO_2 laser contact opening parameters	
Laser parameter	Parameter value
Energy level	1
Attenuation	75 degrees
Lens	L1
Projection mask	3000 x 3000 μm ^{2}
# pulses	10
Pulse repetition frequency	100 Hz
Fluence	13.2 J/cm^2

The use of CO_2 laser for the removal of polymer on top of a metal surface results in a residual polymer layer on the metal layer. This is caused by interference of the incident laser light at the metal surface with the reflected laser light. This phenomenon leaves a polymer layer on top of the metal layer with a theoretical thickness of about 1/4 of the used laser wavelength (= 2.5 μm). In practice, this layer is about 1 μm thick. It can be removed by using an additional Excimer laser ablation step, using the laser parameters of Table 6.13.

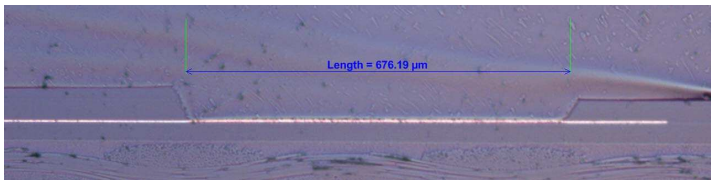


Figure 6.23: Cross-section of a contact pad, opened with CO_2 laser ablation.

Figure 6.24 shows the complete schematic process flow for the opening of embedded contact pads.

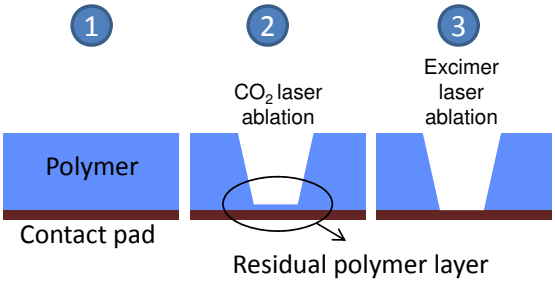


Figure 6.24: Schematic process flow for the opening of embedded contact pads.

Table 6.13: Excimer laser ablation parameters for the cleaning of contact pads after opening with CO_2 laser ablation.

Excimer laser contact opening parameters	
Laser parameter	Parameter value
Puls Energy	4 mJ
Projection mask	3000 x 3000 μm ^{2}
# pulses	3
Pulse repetition frequency	200
Fluence	85 mJ/cm^2

When the contact pads are opened, they become subject to environmental influences like oxygen presence and humidity. Since copper is very sensitive to corrosion, the contact pads should be treated right after laser ablation. A standard procedure is the electroless plating of Ni and the immersion of gold consecutively onto the copper pads. The Ni layer acts as an oxidation barrier for the underlying copper and should be at least 3-5 μm thick. Ni as top finish is not preferable when soldering has to be done on the contact pad, since it shows

poor wettability to solder. The gold coating on the Ni has excellent wettability by molten solder, does not oxidize and does not degrade with time. The 'immersion gold' plating process self-limits at around 0.05 to 0.1 μm , which is beneficial from the cost point of view, but also reduces the possibility of gold embrittlement caused by the formation of a gold-tin intermetallic phase (Tin in solder). The thin gold layer alone would not protect the underlying copper against oxidation.

Figure 6.25 shows pictures and close-ups of contact pads which are (from left to right): Embedded, CO_2 laser opened, Excimer laser cleaned, NI-Au plated and soldered. The close-up of the CO_2 laser opened contact pad, shows rainbow-like colors, which are caused by light interference inside the thin polymer residual layer. These colors are not present in the Excimer cleaned contact pads since the residual layer is removed. The soldering directly on the copper pads was done with standard Pb containing solder at 250 ^{o}C, since the temperature of 300 ^{o}Cneeded for Pb-free solder is too high for the surrounding polymer. Nowadays there are also Pb-free solders available which can be applied at lower temperatures.

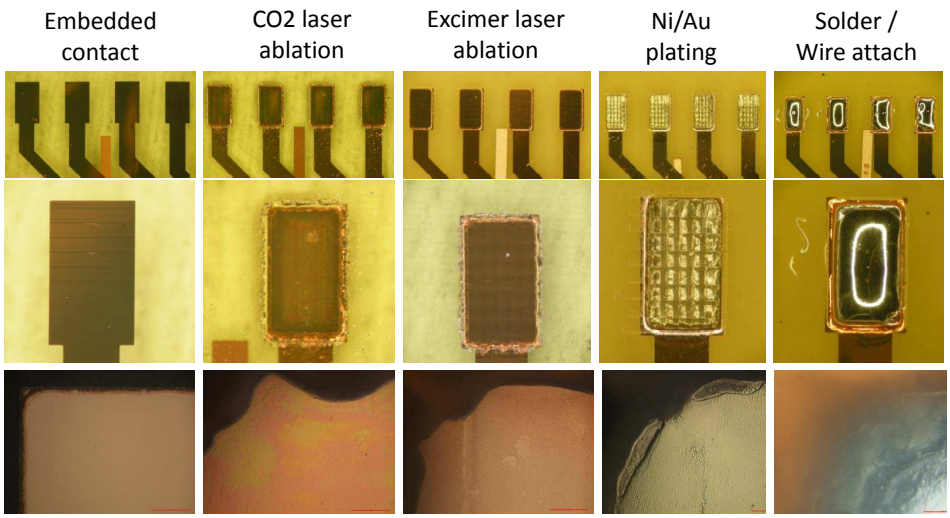


Figure 6.25: Pictures and close-ups of contact pads which are (from left to right): Embedded, CO_2 laser opened, Excimer laser cleaned, NI-Au plated and soldered.

6.5 Embedding of ultra thin IC's

Opto-electronic components like VCSEL's and Photodiodes need the presence of current drivers and amplifiers respectively. Most PCB's also house a lot of other IC's (Integrated Circuits) to introduce extra intelligence into the device. This chapter will investigate the possibilities to embed such IC's inside the same SU-8 layer build-up as the opto-electronic components presented earlier in this Chapter. The embedding of electrical IC's also enables us to measure via- and line- resistances by performing daisy-chain and 4-points measurements.

The thinning of silicon chips - which are usually much bigger in size and thickness than the opto-electronic devices presented in this work - was investigated in the framework of another PhD thesis at CMST [5]. We used those thin IC's as starting point for this section.

Placing of ultra thin IC's is mainly done with pick & place vacuum tools. However, ultra thin chips are very fragile and the yield of most pick & place processes with standard tools are too low.

CMST Microsystems presented a chip placement technique inside a cavity using a mask aligner: The cavity of the substrate is dotted with adhesive. The substrate is then hung upside down in a mask adapted for vacuum holding of substrates, while the chip is placed face down on the movable substrate table of the mask aligner. When aligning is done (under the microscope), the substrate is lowered carefully onto the chip and the drop of adhesive should flow out evenly under the backside of the chip. The substrate can be released from the mask holder and turned over [6, 5, 4]. The same technique was also reported by the Austin University, Texas for the placement of 10 μm thin VCSEL- and photodiode arrays [7].
The latter cavity approach is compatible with the process flow of the embedded optical link, regarding that the heat sink and cavity should have the size of the IC and are consequently a lot larger. The fixing of such a large die inside the cavity needs a good gluing method. The same underfill material as described in Section 6.2.4 was used. Figure 6.26 shows three set-ups for the glue dispensing inside the cavity, together with the result after the hardbake of the glue. We see that a discrete dispensing of a drop in the middle and/or in the corner of the cavity always results in curling of the mounted die (see Fig. 6.26(left) and 6.26(center)). Distributed glue dispensing over 3/4 of the cavity surface (see Fig. 6.26(right)) results in a well fixed, completely flat die.

The chip covering SU-8 layer also shows good covering behavior on top of this large die, as it did for the opto-electronic components. Excimer via ablation, sputtering and fan-out etching is completely similar to the process flow in the Section 6.4.2. Figure 6.27 shows the embedded IC (Fig.6.27(a)) and the Excimer laser ab-

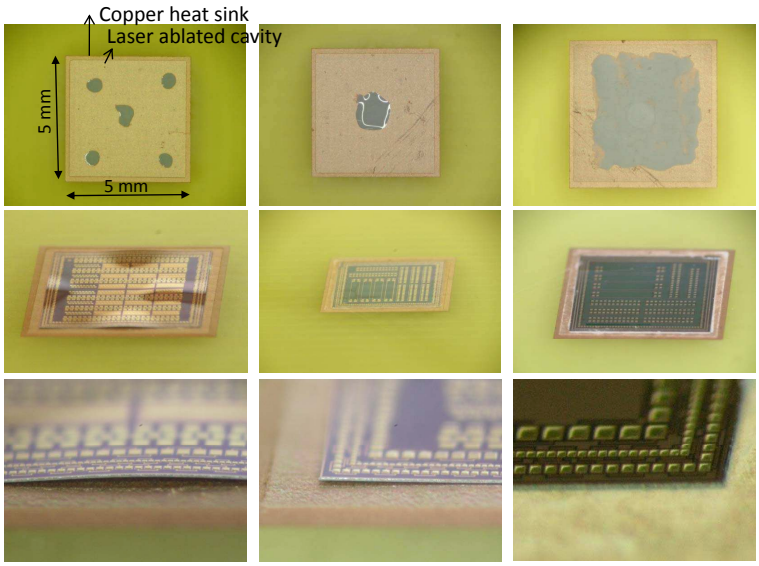


Figure 6.26: Three glue dispensing set-ups inside the cavity (top), together with the result after placement of the IC and the hardbake of the glue (center and bottom).

lated micro-via's (Fig.6.27(b)) after sputtering and after etching (Fig.6.27(c & d)). The via pitch for the used IC is 100 μm .
The edges of the IC contain a daisy chain structure all around the IC. The lay-out of the sputtered metallization tracks also include this structure, which allows us to do daisy chain measurements and 4-points measurements.
The daisy chain includes about 176 via's and can be measured at 4 different points. This allows us to measure the daisy chain resistance distribution over the four quarters of the chain. Figure 6.28 shows the measured resistance values of the four quarters (44 via's each). A difference in value is noticeable, but acceptable. The high resistance value is not due to the via resistance as will be shown with the 4-points measurement, but due to the high resistance daisy chain interconnections on the IC.

4-points measurements consist of driving current through a via, while measuring the voltage over that via. To eliminate the resistance of the tracks towards the via, the current driver tracks and the voltage measuring tracks are different, as is shown schematically and on a photograph in Figure 6.29. Detailed 4-points measurement and daisy chain measurements results can be found in Chapter 8, Section 8.5. The average measured via resistance in SU-8 is about 16.5 mΩ. In [5, 4], similar via-measurements were performed on the same embedded IC, but with Polyimide PI 2611 from HD Microsystems [8] as base embedding material and YAG laser (355 nm wavelength) ablated mirrors. The via's in the optimized

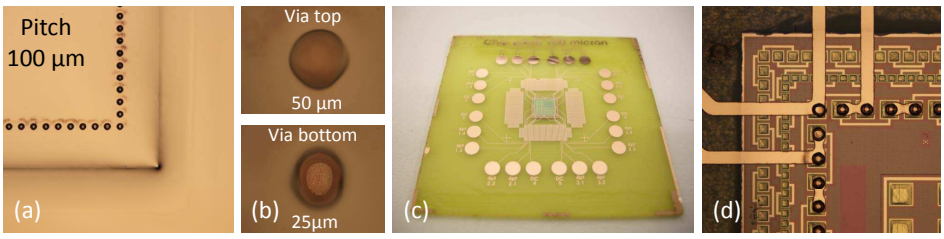


Figure 6.27: Pictures of the embedded IC (a) and the Excimer laser ablated micro-via's (b) after sputtering (a & b) and after etching (c & d).

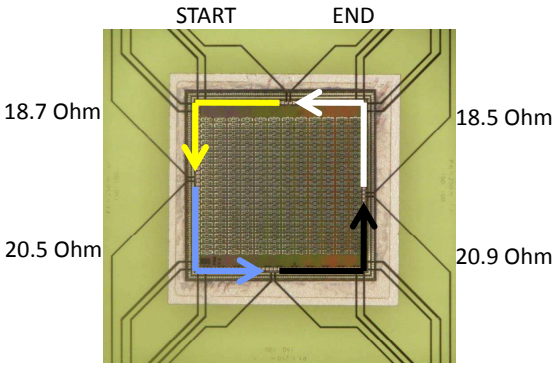


Figure 6.28: Daisy chain resistance measurement for the the four quarters of the embedded die.

samples had an average resistance of 23.2 mΩ.

The measured resistivity of a plain sputtered 1 μm thin copper track is 40 nΩm. When we would assume that the resistivity of the copper in the via is the same as for a plain track, the theoretically resistance of the via should be around 3 mΩ, based on the via dimensions. The measured via resistance is however 16.5 mΩ, which is five times the theoretical value. This is due to the nonuniformity of the copper inside the via and the edges and the roughness of the via side wall roughness. The contribution of the via roughness to the total resistance of the electrical path on the substrate is however negligible. The resistance of the via's is 5 times higher than the resistance of the tracks per unit of length, but the length of the tracks are about 1000 times larger than the depth of the via's.

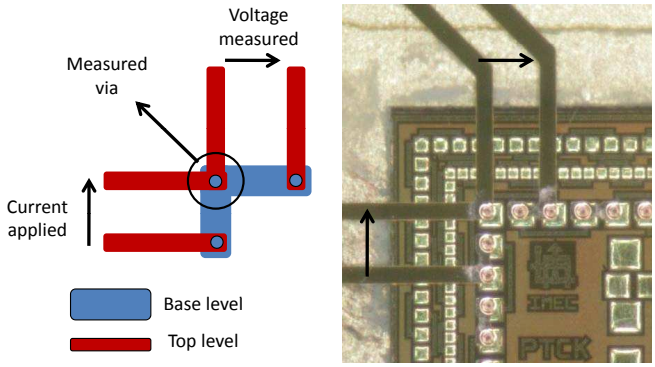


Figure 6.29: 4-points measurement schematic explanation (left) and picture of this principle applied to an embedded IC (right).

6.6 Other embedding materials

In Section 6.4.3, we discussed Truemode™ Backplane Polymer as the embedding material for the opto-electronic components and the local delamination problem, which made us use SU-8 as embedding polymer. In this section we discuss the use of Epocore / Epoclad , LightLink™ and Ormocers® for this purpose.

The Epocore / Epoclad material can be used as a variant to Truemode™ Backplane Polymer since it shows good laser ablation behavior, chip covering properties, etc. The disadvantage of using this material is however the high viscosity of the material, which does not allow us to fabricate layers thinner than 40 μm. The embedded optical link build-up contains a lot of layers, which thicknesses add up really fast if every layer would be minimum 40 μm thick. The Epocore / Epoclad material also showed bad flexibility (see Chapter 4, Section 4.7.2).

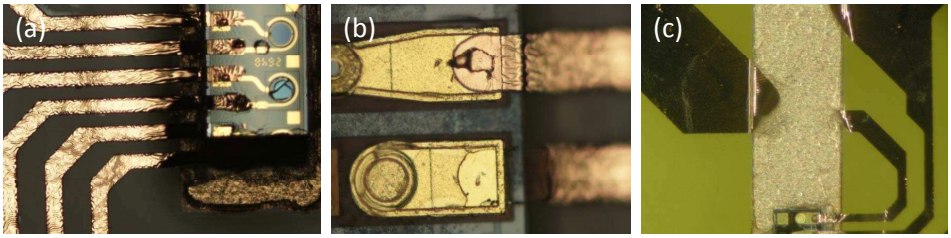


Figure 6.30: Drawbacks of LightLink™ as a chip embedding material.

LightLink™ is an excellent material for the fabrication of waveguides, but it has

a few major drawbacks when it comes to the embedding of components. Figure 6.30 illustrates these issues. First of all, the metallization of a cured LightLink™ surface looks like in Fig.6.30(a). The surface is completely wrinkled after sputtering. A second problem is the chip covering behavior: In Fig. 6.30(b) we can clearly see that a part of the chip covering LightLink™ material has disappeared, probably because of bad adhesion to the chip. Another problem is the fact that the LightLink™ material contracts hydrofobically on top of a plated copper surface (e.g. the heat sink). In Fig.6.30(c) we see that the metallization on top of the LightLink™ is interrupted at the copper plated heat sink, since there is no LightLink™ material on top of the heat sink caused by contraction.

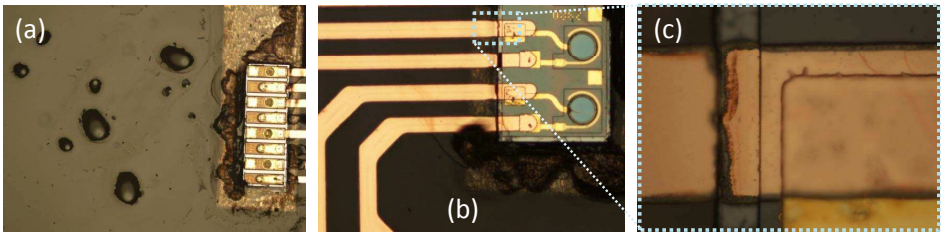


Figure 6.31: Drawbacks of Ormocers® as a chip embedding material.

Ormocers® is vulnerable to the etchants which are used during the etching of the TiW and copper layers. Fig. 6.31(a) shows the defects inside the polymer after etching. This makes metallization of Ormocers® impossible. When Ormocers® is spin-coated on top of a chip, it will contract hydrofobically, leaving the chip uncovered. Direct metallization onto the chip without covering layer is possible as can be seen in Fig. 6.31(b) & (c), but at the interface between chip and polymer, the copper etchants are able to penetrate and etch the copper as can be seen on the close-up (Fig.6.31(c)).

6.7 Conclusions

The embedding of ultra thin (25 μm) opto-electronic components inside the cladding layer of the flexible optical waveguide foil (see Chapter 4) was investigated using different polymers as embedding material. Each embedded chip is provided with a copper plated heat sink and was leveled with the embedding layer, limiting the possible chip tilt angle to lower than 1^o. Laser ablated micro-via's and a sputtered copper layer provide galvanic interconnection towards the embedded chips and fans out the small pitch chip contact pads towards larger contact pads if necessary. These can be opened using different laser ablation steps and can be used for soldering and galvanic contact to the outer world. Together with the opto-electronics, we achieved to embed ultra thin Integrated Circuits

(IC's) in the same layer to enhance the intelligence of the foil. The embedding of IC's also pointed out the low resistance of the laser ablated via's towards the embedded components in SU-8. Finally, the waveguide stack which needs to be fabricated on top can be aligned with a 10 μm accuracy with respect to the active areas of the embedded opto-electronics.

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Chapter 7

Embedding of optical coupling elements

The embedded VCSEL's and Photodiodes presented in Chapter 6 are vertical emitting/detecting opto-electronics, while the embedded waveguides presented in Chapter 4 are a horizontally optical transportation medium. To overcome this, 90 degree out-of-plane coupling elements are needed. These elements have a large contribution to the total optical loss of the system and need to be chosen carefully. This chapter investigates the simulation, fabrication, embedding and characterization of different kinds of coupling elements. Furthermore, optical communication from and to the foil is realized by embedding and coupling of optical fibers in the foil.

7.1 Introduction

Cheap optical sources and detectors within the datacom wavelength of 850nm are often vertical emitting or vertical sensing elements, while the waveguides are positioned horizontally. This issue demands for additional 90 degree optical coupling features.

Optical out-of-plane coupling can be achieved using grating couplers or micro-mirrors. The micro-mirrors have the advantage of being wavelength independent, highly reproducible and can be fabricated with a large variety of technologies such as micro-dicing, V-shaped diamond blade, reactive ion etching, X-ray lithography, laserablation, polishing, etc. In this chapter we will not look into the grating couplers, since their fabrication process is more complicated and less compatible with the proposed process flow of the optical waveguide foil and the embedded opto-electronics presented in Chapter 4 and Chapter 6 respectively.

In this chapter, two micro-mirror fabrication methods are investigated which are able to be performed within the infrastructure of CMST Microsystems: laser ablated micro-mirrors and mirror plugs. Both methods are very different in approach. During laserablation, material of the waveguide is removed in such a way, that the waveguides end up with a 45^o facet. In the mirror plug approach, the waveguides are terminated vertically and an externally fabricated mirror component with a 45^o facet is positioned behind the waveguide. Figure 7.1 shows the difference between the two approaches and a cross-section of the light pad in both cases.

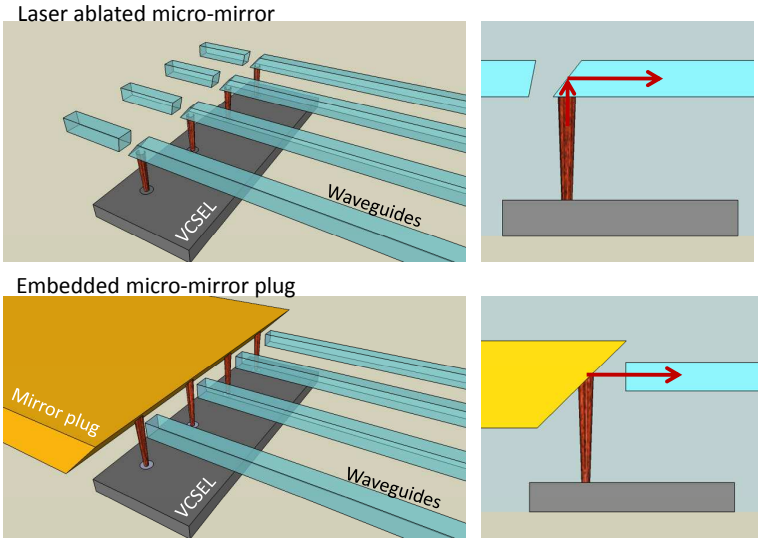

Figure 7.1: Schematic explanation of the difference between the laser ablated micro-mirror and the mirror plug approach.

A study of these two approaches for their use in multilayer waveguide applications can be found in [1]. The work described in this Chapter looks however deeper into the application of above mentioned micro-mirrors inside the embedded optical link. The additional issues which consequently have to be taken into account are as follows:

- Direction of the light coupling: The optical coupling of the light from the waveguides should be done downwards to the embedded opto-electronics below instead of upwards to optical fibers or mounted opto-electronics on the top. This eases the metallization of the mirror since the aimed mirror slope is the opposite of the one aimed in [1], which caused problems.

- Light acceptance elements: In [1], the light is coupled from the waveguide into a waveguide at another level or into an optical fiber, while in the case of the embedded optical link, the light is immediately coupled from a VCSEL active area or to a Photodiode active area. This means that the light acceptance conditions are totally different and that the coupling efficiencies in [1] cannot be used in this work.
- Waveguide material and fabrication method: In [1], Truemode™ Backplane Polymer wet film waveguides are laserablated, while in this work, Truemode™ Backplane Polymer dry film waveguides are used which are fabricated using photolithography.
- Presence of embedded actives: The laser ablated mirror grooves are ablated downwards. The presence of actives underneath the ablation area limits the ablation depth.
- Mirror plug characteristics: When choosing for the embedded mirror plug approach, the plug needs to fulfill additional requirements like flexibility, low thickness and high temperature resistance.

7.2 Ray tracing simulations

The total optical power loss in the embedded optical link has multiple contributors. The loss within the waveguides consists of absorption, scattering and extrinsic losses. These losses can only be minimized by minimizing the waveguide side wall roughness. This is investigated in much more detail in Chapter 3, Section 3.3.3 and Chapter 4, Section 4.7. For more complex optical guiding structures including micro-mirrors, more loss contributors are coming into play due to dimensional misalignments and light beam divergence. Since there are so many dimensional parameters which can be varied inside the optical link, an intuitive approximation of losses is impossible. To minimize the total optical loss of an embedded link, we need to get an idea which dimensional parameters have the highest impact on the loss and try to optimize the process flow with this information.

A large variety of optical design and simulation software is on the market today. A few of these are sequential ray-tracing, non-sequential ray-tracing, Beam Propagation Method and FDTD simulation. The latter becomes useful when the feature sizes in the optical system approach the light wavelength-scale. Since this is not the case in our optical system, we need a ray tracing software. The difference between sequential and non-sequential ray tracing is that the latter permits rays to encounter surfaces in any order and any number of times with automatic ray splitting. Therefore we will work with a non-sequential software.

In what follows, the ZEMAX package was used in non-sequential mode.

The set-up for the simulations is shown in Figure 7.2. The default layer stack consists of a 50 μm thick undercladding layer, a 50 μm thick core waveguide layer and a 50 μm thick uppercladding layer. The VCSEL is modeled as a light emitting circular area with diameter 15 μm and half-divergence angle of 10^o in air and 6.3^o in SU-8. The photodetector is modeled as an 100% absorbing 70 μm diameter circular detecting area. The micro-mirrors are modeled as perfect metal reflectors. The amount of simulated rays is set to 10.000. The length of the waveguide is 2 cm. In the left top corner of Figure 7.2, the X,Y and Z-axis are defined as they will be used in the rest of this section. Only dimensional influences are simulated, no scattering or absorption has been taken into account, since we have no control of these parameters in the fabrication process.

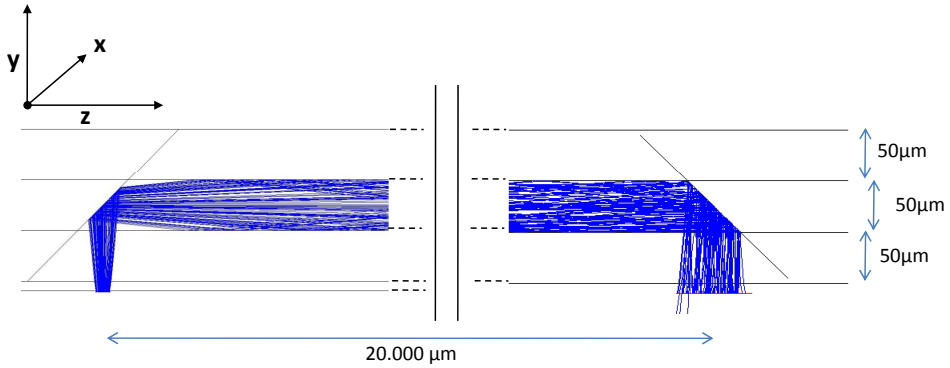

Figure 7.2: ZEMAX ray-tracing simulation set-up for the dimensional optical simulation of the embedded optical link.

Waveguide misalignment

Figure 7.3 shows the optical loss increase for misalignment of the waveguides in the X-direction with respect to active area of the embedded VCSEL's and photodiodes. Four graphs are included: misalignment at the VCSEL side of the link and misalignment at the photodiode side of the link, both in the case of a laser ablated mirror and for an embedded optical plug. The optical loss is slightly more sensitive to a misalignment at the VCSEL side than at the PD side, however a realistic maximum waveguide misalignment of 10 μm (see Table 7.1) still results in losses lower than 1 dB per mirror.

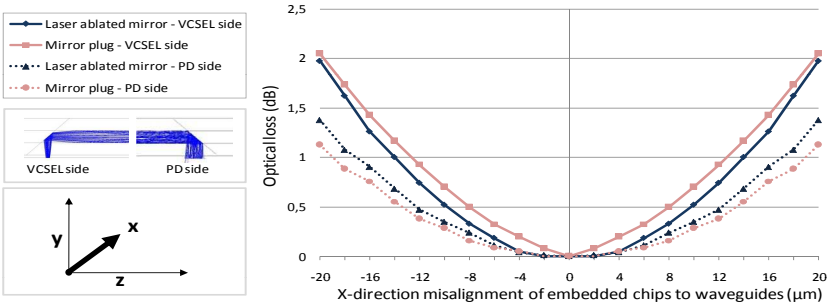

Figure 7.3: Optical loss simulation in function of the X-direction misalignment of the waveguides with respect to the active embedded VCSEL's and photodiodes.

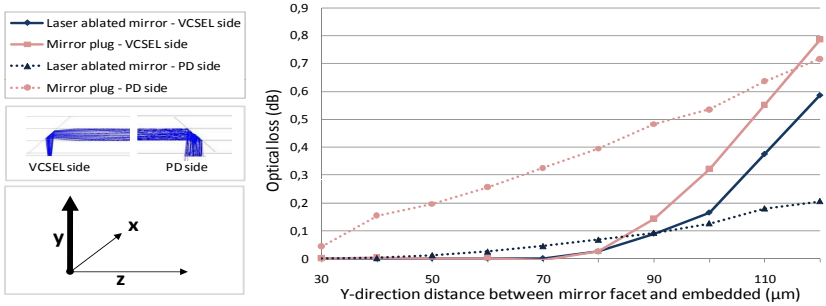

Figure 7.4: Optical loss simulation in function of the Y-distance between the embedded VCSEL's / photodiodes and the corresponding micro-mirrors.

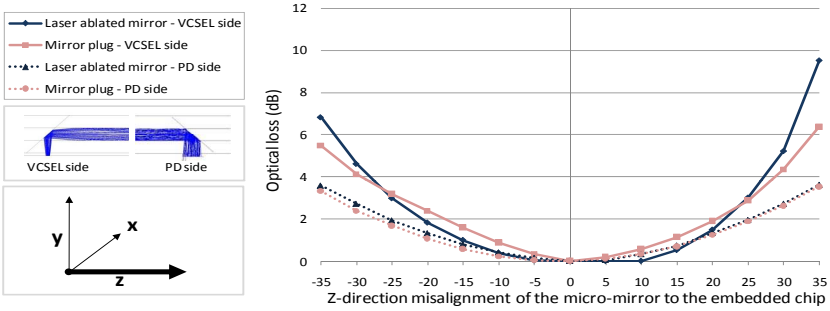

Figure 7.5: Optical loss simulation in function of the Z-misalignment of the micro-mirror with respect to the embedded VCSEL's / photodiodes.

Vertical distance between embedded opto-electronics and coupling mirror

Figure 7.4 shows the optical loss in function of the Y-distance between the embedded VCSEL's / photodiodes and the corresponding micro-mirrors. This distance consists of the SU-8 chip covering layer, the Truemode™ Backplane Polymer isolation layer (see Section 7.5), the Truemode™ Backplane Polymer undercladding layer and half of the thickness of the core layer. The losses are significantly higher at the PD side for the use of a mirror plug. This can be explained by the fact that the light coming out of the waveguide starts diverging immediately. In case of a mirror plug, the light which is coming out of the waveguide has to travel a much longer distance before it reaches the photodetector. In case of a laser ablated mirror, the light is captured inside the waveguide right until it reaches the mirror. The Y-distance between Photodiode and micro-mirror can be realistically upto 90 μm (see Table 7.1), resulting in a loss of 0.45 dB when using a mirror plug.

Coupling mirror misalignment

Figure 7.5 shows the optical loss in function of the Z-misalignment of the micro-mirror with respect to the embedded VCSEL's / photodiodes. The losses are clearly higher at the VCSEL side. The Z-alignment for a laser ablated mirror on top of an embedded VCSEL can be maximum 25 μm (see Table 7.1) which results in a loss of 2.99 dB at the VCSEL side and 1.92 at the photodiode side. For a mirror plug, the misalignment can be controlled below 10 μm (see Table 7.1) resulting in 0.73 dB at VCSEL side and 0.28 dB at photodiode side. The alignment of a laserablated mirror seems to be crucial for the losses, while the experiments show that the alignment accuracy is rather poor (see section 7.3).

Tilt of the embedded opto-electronics

Figure 7.6 shows the optical loss simulation in function of the die tilt angle of the embedded VCSEL/photodiode. In Chapter 6, Section 6.2.4 we concluded that the VCSEL/photodiode can be tilted after mounting in the cavity. This angle is however limited to a maximum of 1^o(see Table 7.1). In the worst case of a mirror plug at the VCSEL side, the additional loss is still limited to 0.06 dB, so negligible.

Horizontal distance between the micro-mirror and the start/end of the waveguide

Figure 7.7 shows the optical loss simulation in function of the Z-distance between the micro-mirror and the start/end of the waveguide. When choosing for the mirror plug approach, there is a certain distance between the micro-mirror and the start/end of the waveguide, where the light is subject to divergence. This

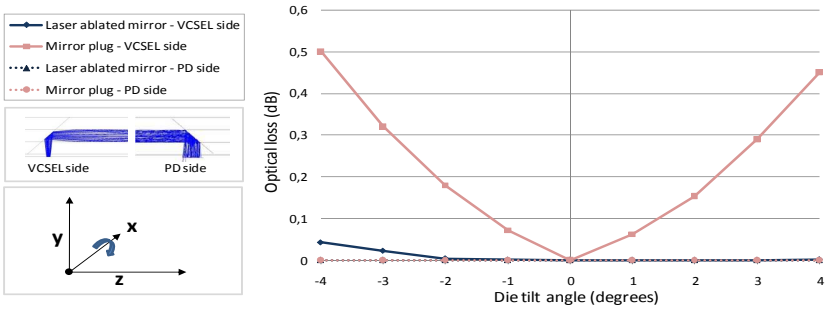

Figure 7.6: Optical loss simulation in function of the die tilt angle of the embedded VCSEL/photodiode.

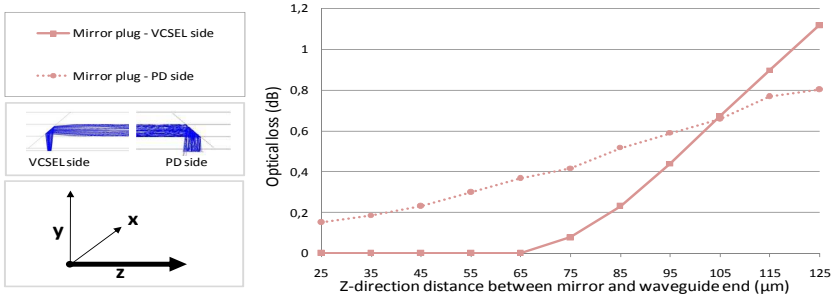

Figure 7.7: Optical loss simulation in function of the Z-distance between the micro-mirror and the start/end of the waveguide.

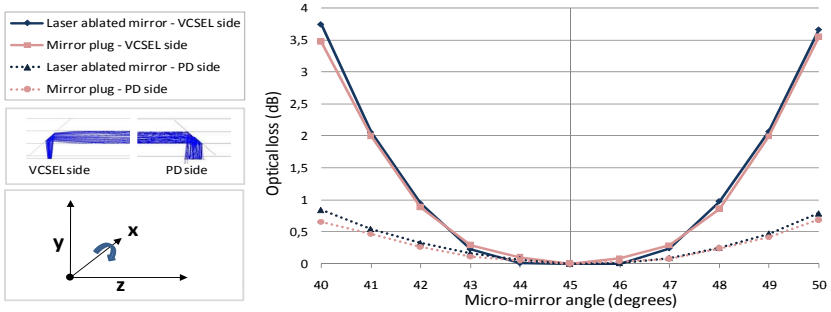

Figure 7.8: Optical loss simulation in function of the micro-mirror angle.

causes extra losses which are not present when using laser ablated mirrors. The maximum experimental distance is about 150 μm (see Table 7.1), resulting in an additional loss of 1.6 dB at the VCSEL side and 0.99 dB at the photodiode side.

Coupling mirror angle deviation

Figure 7.8 shows the optical loss in function of the micro-mirror angle. The loss is most sensitive to the micro-mirror angle variations at the VCSEL side. When using a laser ablated mirror, the angle of the micro-mirror cannot be controlled very well (see Section 7.3). Angle deviations of 5 degrees have been measured (see Table 7.1), resulting in a loss of 3.7 dB at the VCSEL side and 0.81 dB at the photodiode side. The angle of the mirror facet of the mirror plug can be much better controlled down to a deviation of only 1 degree (see Section 7.5), resulting in loss less than 0.1 dB at both VCSEL and photodiode side.

Waveguide cross-sectional dimensions

Figure 7.9 shows the optical loss in function of the waveguide height and width variations. Between 32 μm and 60 μm , the additional loss due to waveguide height or width variations is lower than 0.2 dB. According to the waveguide dimension variations discussed in Chapter 3, Section 3.3.3, the dimensions stay indeed inside this dimension window.

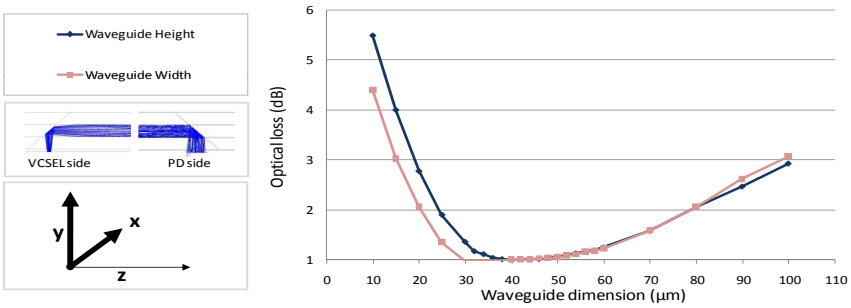

Figure 7.9: Optical loss simulation in function of the waveguide height and width.

The waveguide cross-sectional dimensions in this work were chosen to be 50 x 50 μm ^{2} to be compatible with standard optical fiber core sizes. Figure 7.10, 7.11 and 7.12 show respectively the optical loss in function of the Z-misalignment of the micro-mirror with respect to the embedded VCSEL's, the Z-misalignment of the micro-mirror with respect to the embedded photodiodes and the micro-mirror facet angle at the VCSEL side (all for laser ablated micro-mirrors) for different waveguide dimensions. This to investigate if the 50 x 50 μm ^{2} dimensions are

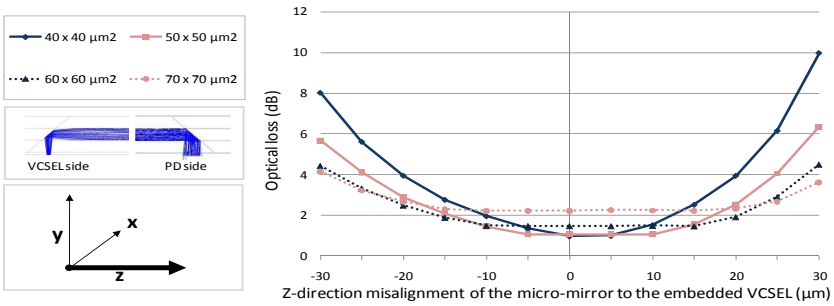

Figure 7.10: Optical loss simulation in function of the Z-misalignment of the micro-mirror with respect to the embedded VCSEL's for different waveguide dimensions.

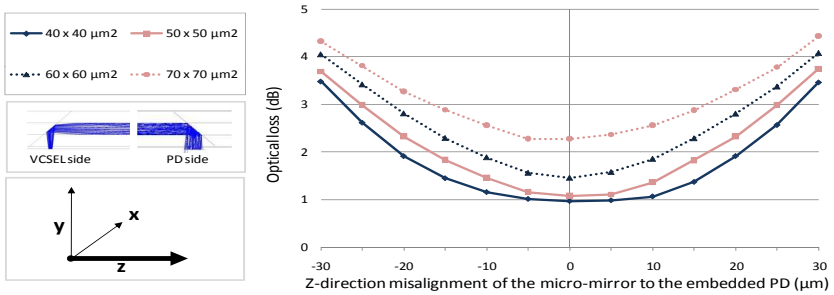

Figure 7.11: Optical loss simulation in function of the Z-misalignment of the micro-mirror with respect to the embedded photodiodes for different waveguide dimensions.

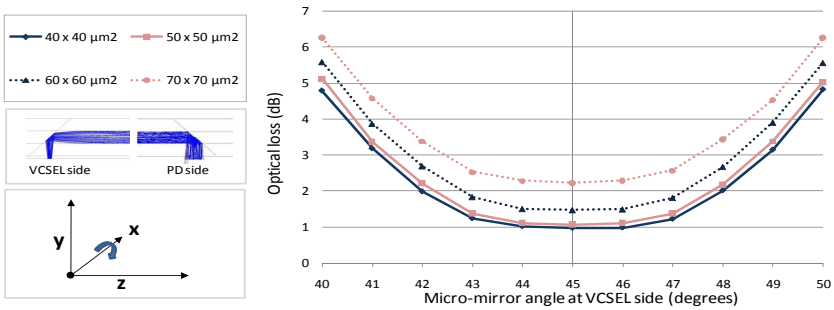

Figure 7.12: Optical loss simulation in function of micro-mirror facet angle for different waveguide dimensions.

indeed the best choice concerning the total optical loss of the embedded optical link. These three graphs were chosen since they represent the three parameters which have the highest impact on the optical loss as proven above.
When the positioning accuracy of the micro-mirror at the VCSEL side (Fig. 7.10) can be controlled within 10 μm , we profit from smaller waveguide dimensions, while a misalignment higher than 10 μm will result in a lower loss penalty for the higher waveguide dimensions.

In Figure 7.11 and 7.12, we see clearly that higher waveguide dimensions result in higher losses. This can be explained by the fact that the beam which exits the waveguide at the photodiode side will be larger for larger waveguide dimensions. Once the light beam is out of the waveguide, the beam will diverge until it reaches the photodetector. The larger the beam is at that stage, the more light will incident next to the 70 μm diameter photodetector active area and be lost. Making the waveguide dimensions smaller than 50 x 50 μm ^{2}, does not result in less losses according to these two graphs.

We can conclude that the 50 x 50 μm ^{2} cross-sectional waveguide dimensions are indeed the optimum choice with respect to the total optical link loss.

Optical loss contributors overview

Table 7.1 shows the optical losses overview, including the "0 dB" parameter values, the experimental worst case parameter values and corresponding worst case optical losses for both the use of laser ablated mirrors and mirror plugs. The experimental worst case values are derived from the research results which is described in Section 7.3, 7.4, 7.5 and Chapter 6. The most significant losses for the use of laser ablated mirrors are due to the Z-alignment of both mirrors and the mirror angle at the VCSEL side, while the most significant loss for the use of mirror plugs is due to the distance between the mirror and the waveguide start/end. The sum of the separate losses is definitely higher for laser ablated mirrors. The optical measurements in Chapter 8, Section 8.2 show that this matches the reality. The simulated total loss in the last line of Table 7.1 is the total simulated loss when all worst case parameter values were inserted in the simulation set-up. The inherent coupling loss is the loss inherent due to the coupling and is independent from the dimensional parameters.

In Section 7.5, the embedding of mirror plugs will be presented, using a laser ablated cavity. The cavity side walls however show tapering, inherent to the CO_2 laser ablation of Truemode™ Backplane Polymer material. The influence of this taper angle of the core-cladding interface is rather limited, because of the small index contrast that exists between the core (n=1.5266) and cladding (n=1.5642) material. The light rays that hit this interface will be refracted according to Snel-

Table 7.1: Optical loss simulations overview, including the "0 dB" parameter values, the experimental worst case parameter values and corresponding worst case optical losses.

Optical loss simulation overview					
Optical loss contributor	"0 dB" value	Experimental maximum value		Experimental maximum loss	
		Laserabl. mirror	Plugged mirror	Laserabl. mirror (dB)	Plugged mirror (dB)
VCSEL-side					
Mirror X-misalignment	0 μm	10 μm	10 μm	0,52	0,7
Y-distance VCSEL to mirror	$\leq$ 75 μm	90 μm	90 μm	0,09	0,14
Mirror Z-misalignment	0 μm	25 μm	10 μm	2,99	0,73
Mirror angle	0 ^{o}	5 ^{o}	1 ^{o}	3,7	0,09
Z-distance mirror-WG	$\leq$ 65 μm	na	150 μm	0	1,6
Chip tilt angle	0	1 ^{o}	1 ^{o}	0	0,06
Inherent coupling loss	na	na	na	0,58	0,65
PD-side					
Mirror X-misalignment	0 μm	10 μm	10 μm	0,34	0,29
Y-distance PD to mirror	0 μm	90 μm	90 μm	0,09	0,48
Mirror Z-misalignment	0 μm	25 μm	10 μm	1,92	0,28
PD-side mirror angle	0 ^{o}	5 ^{o}	1 ^{o}	0,81	0,05
Z-distance mirror-WG	0 μm	na	150 μm	0	0,99
Chip tilt angle	0	1 ^{o}	1 ^{o}	0	0
Inherent coupling loss	na	na	na	0,48	0,48
Simulated total loss				8,42	5,32

lius law of refraction. The incident laser beam will be deviated for 0.75^o if the taper angle is 29^o like it is in the cross-section in Figure 7.13. This deviation is acceptable when we take the results from Figure 7.8 into account.

7.3 Laser ablated micro-mirrors

The use of laser ablation for the fabrication of optical micro-mirrors introduces some advantages compared to other techniques: laser ablation is used a lot in the process flow of the embedded optical link for the realization of cavities and micro-via's. Thereupon is the Truemode™ Backplane Polymer material an excellent material to be ablated with few to no debris and very smooth ablated surfaces. There is also a lot of knowhow on the ablation of Truemode™ Backplane Polymer within the CMST Group, stated in the PhD thesis's [1] and [2]. The ablation of mirrors on top of embedded actives however adds some extra challenges to the previous work, itemized in Section 7.1. Laser ablation also has the advantage to be very fast and it almost doesn't interfere with the rest of the process flow, since it is a dry, room-temperature process at the far end of the process flow.

Two different laser ablation mirror fabrication approaches are investigated: tilted laser ablation and distributed laser ablation. The difference of the two approaches

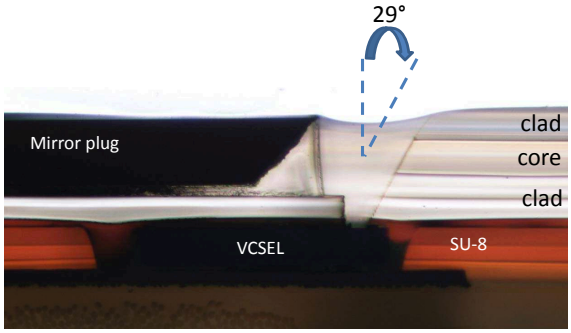

Figure 7.13: Cross-section of an embedded VCSEL array and mirror plug, showing the taper angle of the laser ablated mirror plug cavity side wall.

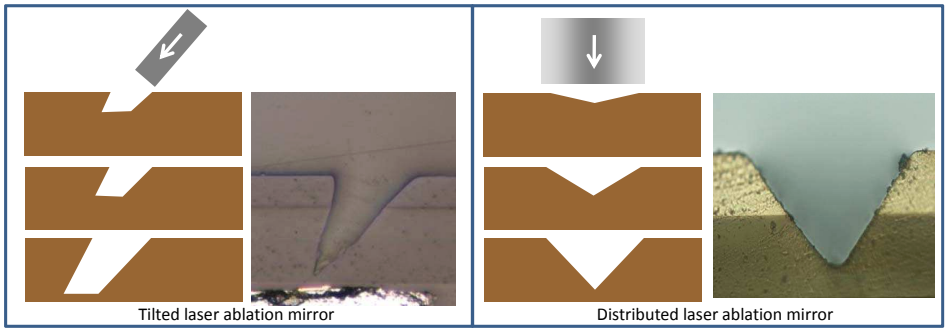

Figure 7.14: Schematic comparison and cross-sections of the tilted laser ablation mirror and the distributed laser ablation mirror.

is explained schematically and with cross-sections in Figure 7.14. The tilted laser ablation consists of tilting the optics from the beam delivery unit on the laser set-up in such a way that the laser beam will incident the Truemode™ Backplane Polymer surface under an angle which can be controlled with an accuracy of 0.5 degrees using a micro-screw. The distributed laser ablation is performed using a triangular shaped beam. Dynamic ablation with such a shaped beam results in a V-groove. By controlling the depth of the V-groove, we can control the angle of the side walls of the V-groove.

During the research of laser ablated micro-mirrors above embedded opto-electronics, we encountered three major technological problems, which will be discussed in what follows.

Ablation depth control

The mirror trench needs to be ablated through the complete uppercladding layer and the waveguide core layer, while it cannot reach the embedded chip underneath the undercladding layer. This means that the process window is quite narrow. Therefore we should have enough control over the trench depth. To test the ablation depth reproducibility, we ablated 9 identical trenches on different periods during the research. The optimum laser power and pulse repetition frequency are 6 mJ and 200 Hz ([2]&[1]), which were optimized in function of the mirror facet roughness. The trenches were ablated using these parameters and a sample translation speed of 100 μm /s with the tilted laser ablation approach. The result is shown in Figure 7.15. The depth can vary upto 15 μm and this just for a 45 μm deep trench. The depth variation for a 120 μm deep groove will even be larger (through the uppercladding and the core layer). The reason for this poor depth control is found in the delivered laser beam power stability over time.

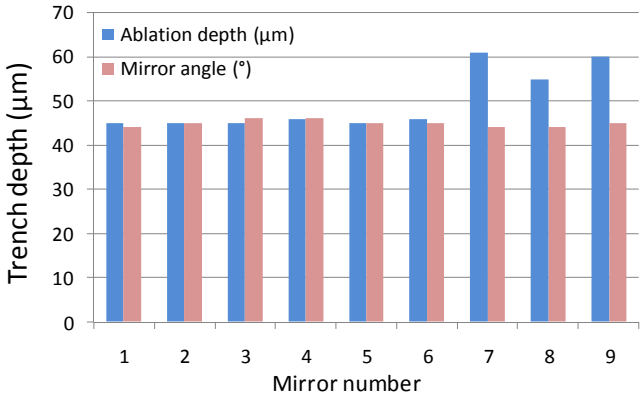

Figure 7.15: Laser ablated mirror trench depth reproducibility (left) and depth in function of the sample translation speed (right).

The poor depth control can result in damaging the embedded opto-electronics which is unacceptable.

Taper differences between core and cladding material

The laser ablation behavior of the core material is different from the ablation behavior of the cladding material. More specific, core and cladding have another taper angle. This causes problems since the core and surrounding cladding layer are ablated in the same ablation process. To get a better view on this problem, we made a cross-section at the edge of a waveguide, so that we can compare the

core and cladding cross-sections in one picture. The deepest trench part is at the cladding (between two waveguides) location and the shallowest at the waveguide location. The trench side wall is much flatter for the cladding part than at the waveguide locations and the difference in mirror angle is about 18^o between the two cases. At the waveguide side walls, there is a transition between the two ablation behaviors, meaning that the actual waveguide mirror surface is rather curved than flat. The non-flatness of the mirror results in a bad coupling efficiency.

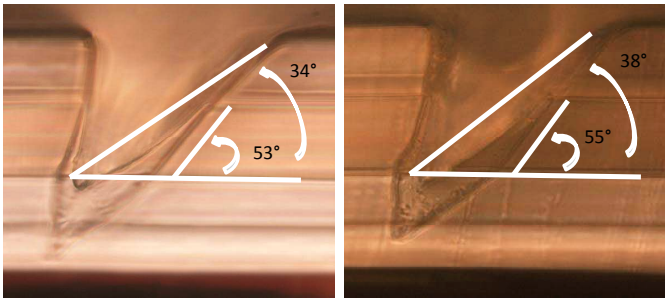

Figure 7.16: Cross-section of tilted laser ablation mirror trench, showing the different taper angle for the cladding and core material.

Dependency on the uppercladding thickness

A third drawback of the laser ablated mirror is the dependency of the mirror positioning to the uppercladding thickness, when using the tilted laser approach. As seen in Chapter 3, Section 3.3.4, the uppercladding layer thickness (consisting of two spincoated Truemode™ Backplane Polymer cladding layers) shows a variation of $\pm$ 10 μm . This results in a 10 μm misalignment of the mirror facet with respect to the underlying embedded opto-electronic component. Figure 7.17(left) shows this principle. During alignment of the laser ablated mirror, the edge of the mirror trench is aligned with the active areas of the embedded VCSEL/PD, with a fixed off-set of (X+Y), so that the middle of the waveguide mirror facet will be positioned right above the active area of the embedded chip (in average). However, if the uppercladding layer thickness (X) is a bit higher than average, the Y-value will be smaller, since (X+Y) is a fixed distance. The Y-distance should be exactly half the height of the waveguides when perfect alignment is aimed. Any change in the Y-value means a misalignment of the mirror. The maximum misalignment of the mirror is the maximum deviation of the uppercladding layer thickness + half of the maximum deviation of the waveguide height + the inherent positioning error due to the limitations of the visual system of the laser. Experimental statistics show that this misalignment can be upto $\pm$ 25 μm , which results in

high losses (see Section 7.2). Figure 7.17(right) shows the X value (uppercladding thickness above the waveguide) for 8 different samples and the consequence of the X-variation for the Y-variation. Y should be 25 μm for a 50 μm high waveguide.

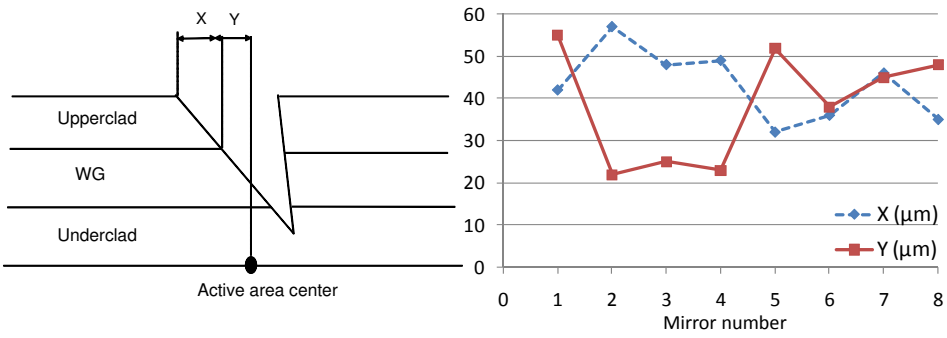

Figure 7.17: Misalignment of the laser ablated mirror with respect to the embedded actives due to the variation in uppercladding layer thickness.

To summarize, the advantages and disadvantages of the distributed laser ablation micro-mirror versus the tilted laser ablation are discussed below, considering the main drawbacks of the laser ablation of micro-mirrors shown above.

- The poor depth control is more problematic when using the distributed laser ablation approach. The depth of the groove defines the angle of the mirror facet. Therefore this approach is only profitable when the delivered laser beam power is well controlled.

- The main advantage of the distributed laser ablation is the flat mirror surface. The different taper angles for core and cladding results in a curved waveguide mirror facet for tilted laser ablation. Using the distributed laser ablation set-up, we ablate from the top, so that the final mirror facet is now actually more the groove bottom than the groove side wall (as in tilted laser ablation). This means that the tapering does not manifest itself, resulting in completely flat groove side walls and a flat waveguide mirror facet.

- The mirror misalignment due to uppercladding thickness variations is occurring in both approaches.

7.4 Pluggable mirror fabrication

The optical simulations in Section 7.2 have pointed out the importance of the micro-mirror positioning and facet angle for the total optical loss of a fully embedded optical link. The use of laser ablation for the fabrication of micro-mirrors inside the waveguides, has shown some detrimental disadvantages (see Section 7.3) according to the mirror positioning, angle and flatness. This section investigates a completely different approach by fabricating a discrete component with a 45 degree mirror facet. By creating the mirror component independent from the optical link fabrication, we have full control over the mirror facet roughness and angle. The positioning of the micro-mirror is then purely subject to the accuracy of the mirror component placing. Using a fine pitch pick and place tool, accuracies below 5 μm are achievable. Manual placing of the components results in an accuracy of 10 μm (see Section 7.5).

In Section 7.5, the embedding of the mirror plug inside the layer build-up using a cavity approach is discussed in detail. This section focuses on the fabrication of the mirror plug.

7.4.1 Deep proton writing (DPW)

The Deep Proton Writing (DPW) technology is a rapid prototyping technology for the fabrication of micro-optical modules [3, 4], developed by the TONA Group at the Vrije Universiteit Brussel (VUB). During DPW, the polymer samples are bombarded with swift protons, which will result after chemical processing steps in high quality micro-optical components. This technique is furthermore compatible with low-cost mass-replication techniques such as micro-injection moulding and hot embossing. The prototype was fabricated in PMMA typical for the DPW technology. Figure 7.18 shows such a prototype mirror plug cut out in a 500 μm thin PMMA sheet (Fig. 7.18(bottom)), a SEM picture of a released mirror plug (Fig. 7.18(top left)) and a gold coated version (Fig. 7.18(top right)). The obtained mirror facet has a surface Ra roughness of 13.4 nm, averaged over 5 random measurements [1].

The use of DPW results in a highly smooth mirror plug facet with very accurate dimensions and mirror angle which can be replicated low-cost and high mass. The disadvantage is the limitation to the proton writing depth. This means that the width of the mirror plugs is limited to 500 μm , which can only cover a 1 x 2 VCSEL or PD-array, while we aim at a highly scalable process upto 1 x 4 and 1 x 12 arrays.

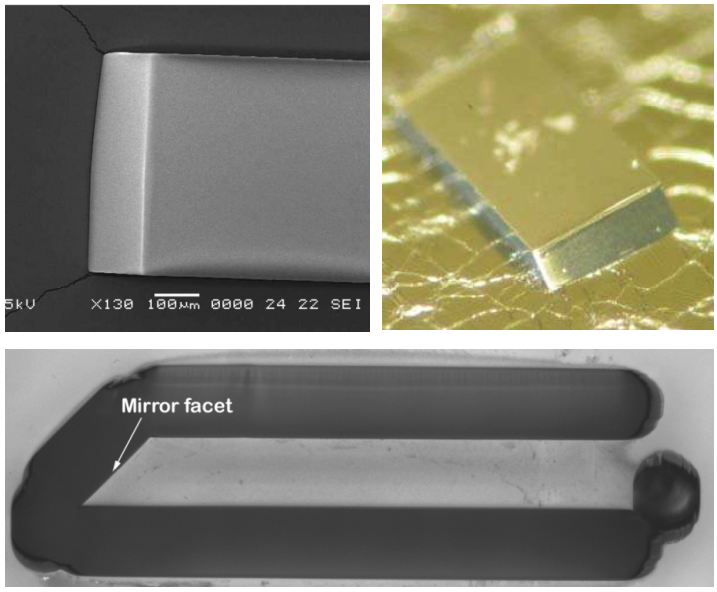

Figure 7.18: Mirror plugs fabricated with the use Deep Proton Writing (DPW).

7.4.2 45 Degree polishing

Due to the lack of scalability of the Deep Proton Writing approach for the fabrication of the mirror plug, a new fabrication technology was developed: 45 degree polishing. The schematic process flow for the 45 degree polishing is shown in Figure 7.19. The material for the mirror plug is chosen to be Polyimide because of its high thermal stability and flexibility. We start from a mother piece (eg. 1 x 2 cm^2) of 500 μm thick PI wafer [5] and clamp it in a special designed polishing tool. Pictures of this tool are shown in Figure 7.20. It consists of a block of PMMA material which was cut into two pieces at an angle of 45 degrees.

These two blocks are then provided with screws to clamp them together and guiding pins to assure that the two blocks can only move horizontally with respect to each other. The PI waferpiece is clamped inside this tool in such a way that it protrudes for a few tens of microns out of the PMMA tool.

A same piece (dummy) of PI wafer is clamped on the other side of the clamping tool trench as is shown in Figure 7.21, to prevent incorrect clamping. The samples in Fig. 7.21(a)&(c) are clamped correctly, while the sample in Fig.7.21(b) is clamped incorrectly. The whole PMMA polishing tool with the clamped PI waferpiece is then polished on rotation polishing paper and polishing cloths. Large grain polishing paper is used first to make sure the two PMMA blocks of the 45 degree polishing tool are perfectly planar. Lowering the grain size in every

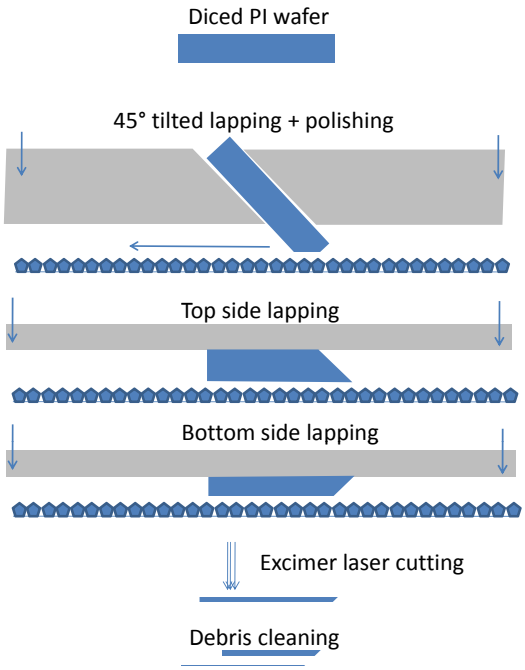

Figure 7.19: Schematic process flow for the fabrication of mirror plug components.

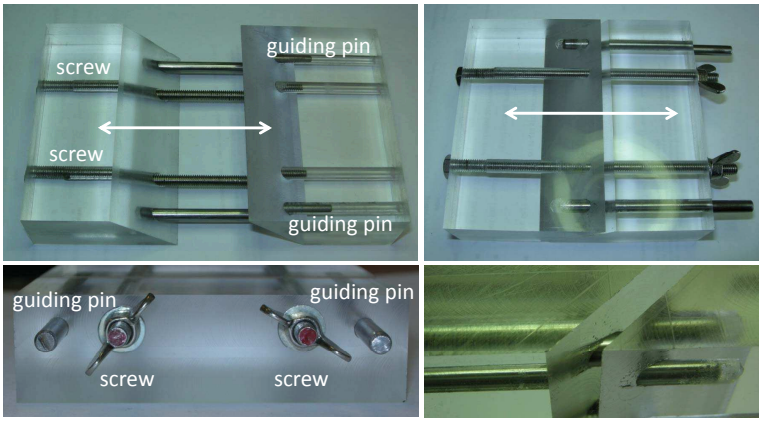

Figure 7.20: 45 degree mirror plug polishing tool.

next polishing step, reduces the mirror facet roughness to a minimum. The last polishing step is done with a 0.3 μm Al_2O_3 grain slurry on a soft polishing cloth.

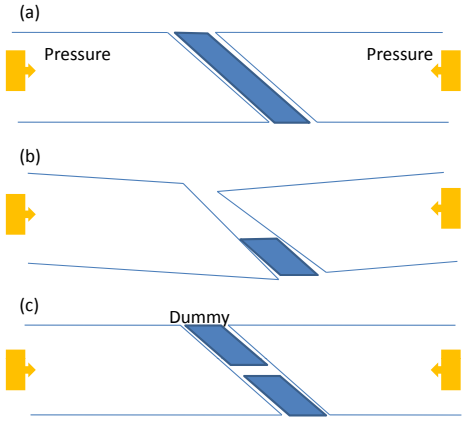

Figure 7.21: Dummy approach for the correct clamping of the mirror plug motherpiece in the PMMA 45 degree polishing tool.

The resulting mirror facet is shown in Figure 7.22(left), together with a WYKO optical non-contact profilometer plot of the surface (Figure 7.22(right)). The Ra roughness of the mirror facet, measured on an area of 50 x 50 μm ^{2} is 13.5 nm, which is well below 1/10 of the used light wavelength (850 nm / 10 = 85 nm). The edges of the 45 degree mirror facet of the motherpiece are a bit rounded due to the polishing and show higher roughness. These side effects are eliminated by lapping the motherpieces at both sides (top and bottom) until it has the aimed thickness of 100 μm (see Fig.7.19). The lapping process and parameters are the same as for the lapping of the opto-electronics in Chapter 5, Section 5.4.3. The roughness of the top and bottom side is not important. The wax mounting step however is crucial to assure perfect parallellism of the motherpiece and thus respecting the 45 degree angle of the mirror facet.

The last step consists of the laser cutting of the mirror plugs out of the motherpiece. The dimensions of the mirror plug should be 1000 * 2000 μm ^{2}, what means that a motherpiece with a length of 2 cm results in 20 mirror plugs. The proposed fabrication method is thus highly scalable. Figure 7.23(a) shows the sideview on the mirror plug and (b) a close-up on the mirror facet. The software-based measurement of the angle shows an angle of 44.46 degrees. Every mirror plug measured this way had a mirror facet angle within a 45 $\pm$ 1 degree range.

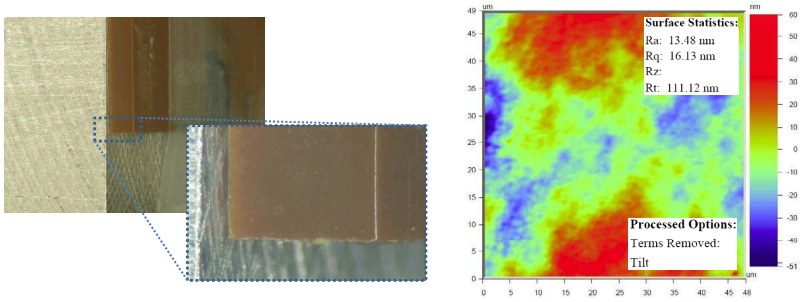

Figure 7.22: Picture of the mirror facet on the PI motherpiece (left) and a WYKO optical non-contact profilometer plot of the mirror surface (right).

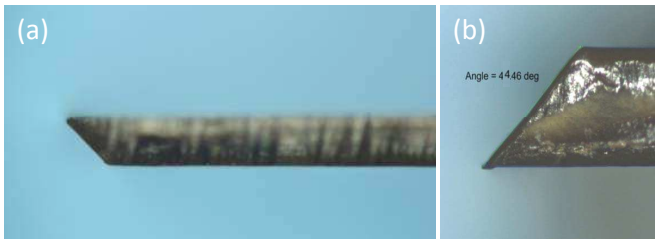

Figure 7.23: Sideview on a mirror plug (a) and close-up on the mirror facet (b).

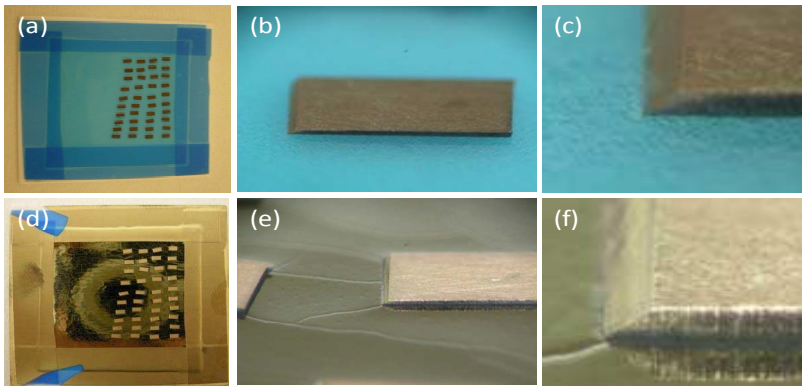

Figure 7.24: Pictures of mirror plugs mounted on a blue low-tac tape before metallization (a,b & c) and after metallization (d,e & f).

For the metallization of the mirror facets, the mirror plugs are mounted on a low-tac tape for handling during the vapor deposition process. A gold layer of 120 nm is deposited. Figure 7.24 shows pictures of the mirror plugs mounted on the blue low-tac tape before metalization (a,b & c) and after metallization (d,e & f).

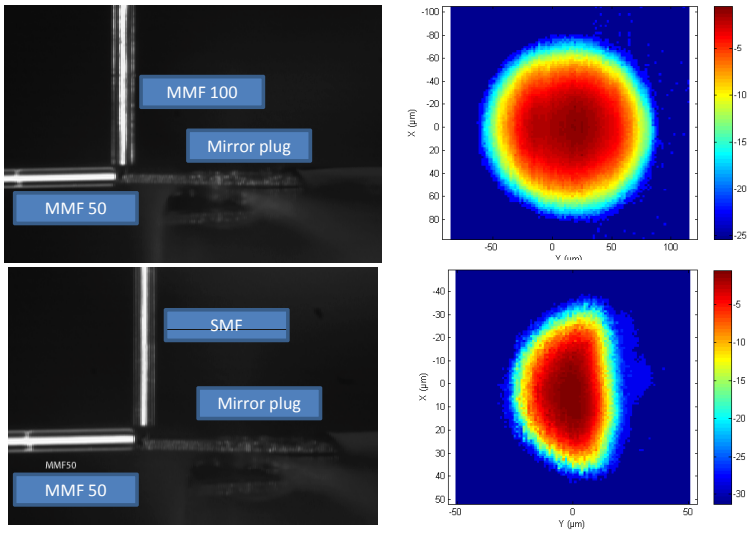

Figure 7.25: Coupling efficiency measurements CCD camera pictures (left) and tolerance plots for the detecting fiber scan (top right) and the emitting fiber scan (bottom right).

The surface roughness of the mirror facet - though very low - causes optical loss, together with the not perfect reflecting gold layer. To quantify the real coupling losses of the mirror, the set-up shown in Figure 7.25 was used. An optical fiber is positioned horizontal and emits 850 nm wavelength light onto the mirror facet. Another fiber is positioned vertically to collect the mirror reflected light. The ratio between the emitted and the detected light defines the coupling efficiency of the mirror. When using a multimode emitting fiber with core diameter 50 μm (NA = 0.2) and a detecting multimode fiber with core diameter 100 μm (NA = 0.29), we measure a maximum coupling efficiency of 88,5% or a coupling loss of -0.529 dB. When using a singlemode emitting fiber with NA = 0.13 and a detecting multimode fiber with core diameter of 50 μm (NA = 0.13), we measure a maximum coupling efficiency of 89,1% or a coupling loss of -0.502 dB. The measurements were performed in the lab of the TONA Group at the Vrije Universiteit Brussel (VUB). A CCD camera shot of both measurements is shown in Figure7.25(left). Figure 7.25(right) shows the tolerance plot for a scan of the detector fiber in the first measurement (top right) and for a scan of the emitting fiber in the second measurement (bottom right).

7.4.3 Wire Electric Discharge Machining

A third investigated fabrication method is the use of Wire-EDM. EDM (Electric discharge machining) is a manufacturing process whereby a certain shape of an object is obtained by using electrical discharges. The material removal from the workpiece occurs by a series of rapidly recurring current discharges between two electrodes, separated by a dielectric liquid and subject to an electric voltage. In case of Wire EDM, one electrode is the workpiece itself and the other electrode is a feeded wire. This is a very fast and cheap way for fabricating components with accurate dimensions. The roughness of wire-EDM cuts side walls is too high to be used as mirror facet. We can however use a pre-polished workpiece and cut along the length of the mirror plug component. Following work was performed at the PMA Group of the Katholieke Universiteit Leuven (KUL).

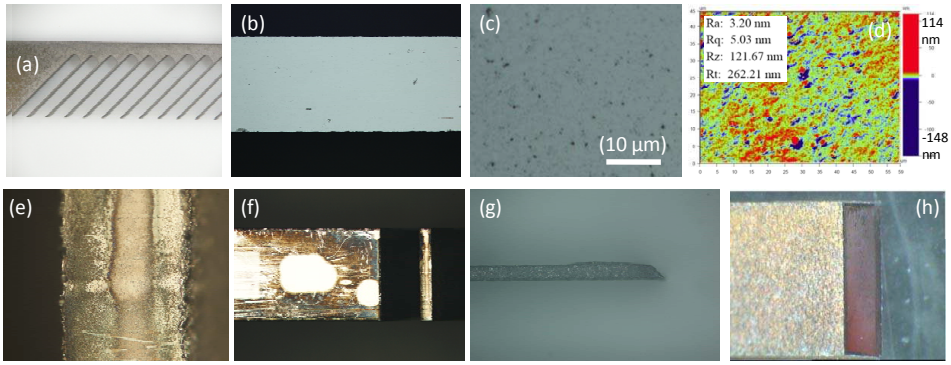

Figure 7.26: Pictures and measurements of Wire-EDM fabricated mirror plugs.

Figure 7.26(a) shows the wire-EDM cuts inside a 1 mm thick tungsten carbide workpiece. The strips that can be seen are the mirror plugs in side view. The end facets of the strips are the 45 degree mirror facets. Figure 7.26(b) shows a picture of the polished side of the workpiece far away from the wire-EDM cuts (several mm) and Figure 7.26(c) a microscopic view on this surface. A lot of black specks are visible, which origin from the wire-EDM cut. Figure 7.26(d) shows a WYKO optical non-contact profilometer measurement of this surface on an area of 45 x 60 μm ^{2}, showing a 3.2 nm Ra roughness. Close to the wire-EDM cuts we see a lot of dirt being deposited on the polished surface, which can however be cleaned with CO_2 laser ablation. Figure 7.26(f) shows a picture of this dirt and a few laser ablated areas (white spots). On the very edge of the cut, we see another phenomenon (Figure 7.26(e)): The polished surface seems modified, probably due to the heat generated in the tungsten carbide during the electric discharges. The use of a more sophisticated wire-EDM machine can reduce the modified area significantly as can be seen on Figure 7.26(h). Since only the middle of the

mirror facet will actually be reflecting light once embedded, the small side strips of modified tungsten carbide will not interfere with the optical pad.

The major drawback of the Wire-EDM is however the limited choice of materials for the workpiece and thus for the mirror plug. Tungsten carbide is not very flexible, even when it is only 100 μm thin. Also the dirt deposition on the polished surface is a problem which needs to be controlled. Trials have been done to use thin copper sheets and electrical conductive paste to temporary protect the polished surface, without success so far. The protecting layers are always flushed away by the electrolyte fluid.

7.5 Embedding of pluggable mirrors

When using laser ablated micro-mirrors, the embedding takes place as one of the last process step in the realization of embedded optical VCSEL-PD links. Therefore this kind of mirror does not have a large impact on the process flow. The use of an externally fabricated mirror plug, on the contrary, introduces large adaptations in the process flow. In this section we will mainly focus on the process flow to embed these mirror components into the layer build-up. Figure 7.27 gives an overview of the dimensions of the mirror plug and a few pictures. The component is 100 μm thick to fit into a cavity inside the waveguide stack and is 2 mm long and 1 mm wide.

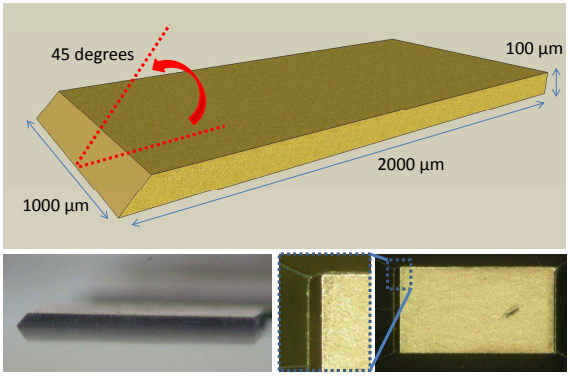

Figure 7.27: Overview of the dimensions of the mirror plug (top) and mirror plug pictures (bottom).

A schematic cross-sectional process flow is shown in Figure 7.28.

The angle of the mirror facet of the mirror plug is crucial and consequently any tilt of the component results in a wrong mirror facet position angle. Therefore

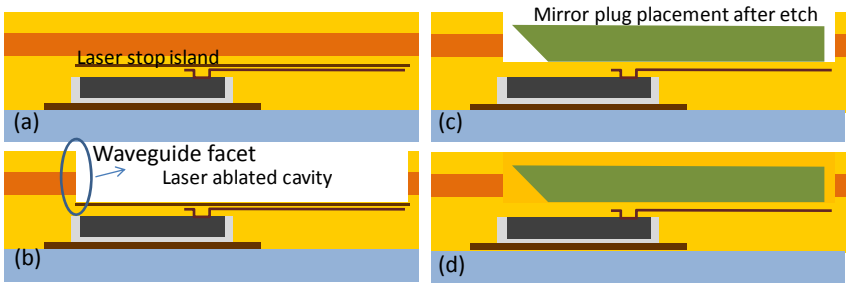

Figure 7.28: Schematic cross-sectional process flow for the embedding of mirror plugs into the layer build-up of the embedded optical link.

we need to be sure the component is placed perfectly flat. This is accomplished by using the same cavity approach as presented in Section 6.2.3. For the use of laser ablation we need a metal stop layer. This layer should be applied after the chip embedding and before the waveguide stack fabrication. The galvanic interconnection layer of the embedded chip is also at that level, so we need an isolation layer. In practice, this means that a thin Truemode™ Backplane Polymer cladding ($\pm$ 7 μm) layer is fabricated on top the fan-out before applying the metal laser stop layer for the mirror plug cavity. Fig. 7.28(a) shows were the laser stop layer is positioned. The laser ablation of the cavity is done similarly to the opening of the contact pads in Section 6.4.4, using the same parameters. The only difference is the waveguide facet (Fig. 7.28(b)), which should be as smooth as possible since it is a part of the light pad of the optical link. The ablation of this facet is done dynamically in one single ablation and as last ablation step of the cavity, so no debris will be deposited on the facet afterwards. After fabrication of the cavity, the metal floor of the cavity is removed by wet etching. Figure 7.29(a) shows an embedded VCSEL with fan-out before application of the laser stop layer, Fig. 7.29(b) shows the laser stop island for the mirror plug cavity, Fig. 7.29(c) after wet etching of the cavity floor and Fig. 7.29(d) a close-up on the waveguide facet.

The placement of the mirror plug is done similar to Section 6.2.4 with the same underfill material. The glue can however not be spread into the light pad. Therefore we spread the glue manual away from the active areas from the embedded chips and be careful when placing the mirror plug. A better solution would be the use of low viscosity thin transparent glue, but we did not finish this research within the time frame of this PhD work. The manual placement of the plug is eased because of the low viscosity glue. This allows us to push the plug very softly into place, reaching an assumed 10 μm positioning accuracy under the microscope. Figure 7.30 shows pictures of the dispensing of the glue Fig. 7.30(a), the manual spreading of the glue Fig.7.30(b), the placing of the mirror plug Fig.

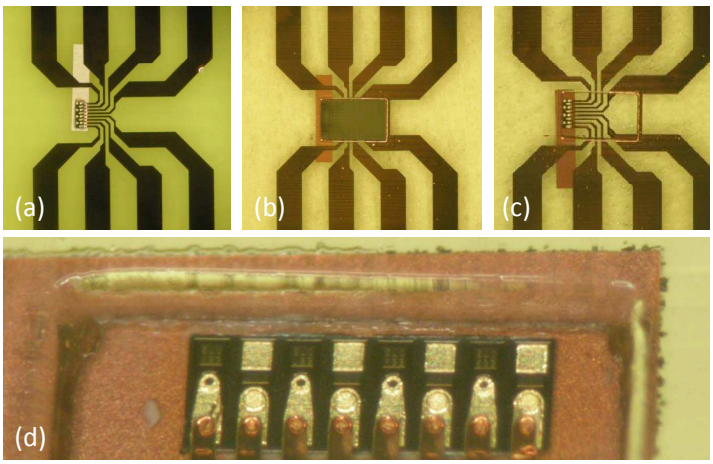

Figure 7.29: Picture of an embedded VCSEL with fan-out layer (a), of the laser stop island for the mirror plug cavity (b), of the cavity after wet etching of the cavity floor (c) and of a close-up on the waveguide facet (d).

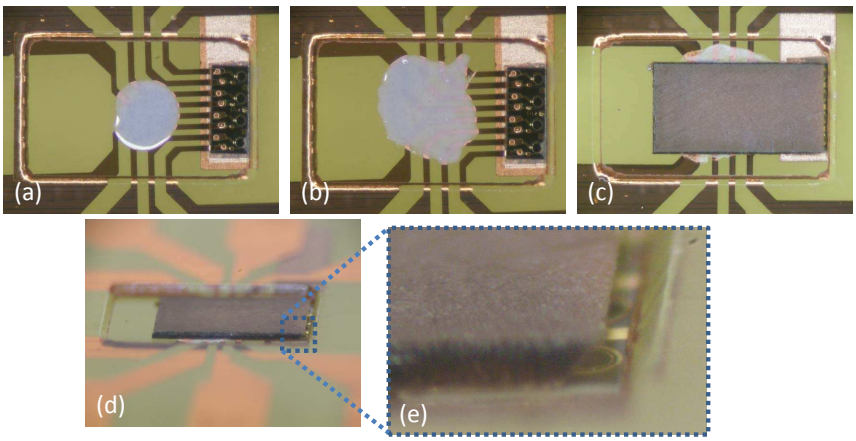

Figure 7.30: Pictures of the dispensing of the glue (a), the manual spreading of the glue (b), the placing of the mirror plug (c) and a close-up (d) & (e).

7.30(c) and a close-up Fig. 7.30(d) & (e).
After heat curing of the glue, a final Truemode™ Backplane Polymer layer is applied to cover and embed the mirror plug and to fill any air gaps next to and underneath the mirror plug. Figure 7.31 shows cross-sections of a completely embedded mirror plug. Fig.7.31(a) shows that the mirror plug is slightly tilted at the mirror facet side. This is caused by the fact that we did not want to put a lot of

pressure on the mirror plug at that end, since we did not want glue to be spread onto the mirror facet. Further fine tuning of the mirror plug placement or the use of transparent glue can eliminate this issue. The tilting is limited though to 1^o. Fig.7.31(b) shows that the alignment of the mirror plug is satisfactory. Optical measurements in Chapter 8, Section 8.2 will proof that the mirror plug alignment is indeed within the requirements.

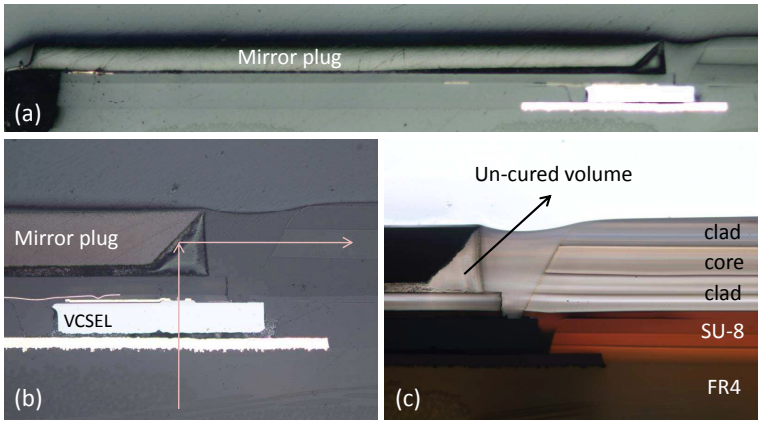

Figure 7.31: Cross-sections of a fully embedded mirror plug above an embedded VCSEL array.

An additional problem however can be seen Fig. 7.31(b) & (c). Since the negative slope of the mirror facet of the mirror plug, the Truemode™ Backplane Polymer underneath the mirror facet is not exposed to UV light during the UV-exposure process step. This results in an uncured material volume at that place. Tilted UV exposure solved this problem but slightly complexes the UV exposure step.

7.6 Coupling of optical fibers to the flexible optical waveguide foil

The opening of the embedded contact pads allows us to communicate to the outer world electrically by means of wire bonds or probes etc. The optical communication to the outer world on the other hand can be done vertically since the VCSEL's emit vertically and the photodiodes detect vertically, but alignment will be crucial. A well established, pluggable optical communication medium is the optical fiber. If we succeed to integrate and couple optical fibers with the embedded waveguides of our optical waveguide foil, we can seriously higher the functionality of the foil, which increases the amount of possible applications. The study on this matter, described in this section, is limited to the proof of principle.

The use of dedicated pluggable connectors on rigid opto-electronic boards has been reported many times as an easy, cheap and effective way to connect optical fibers to the board. However, the optimization and fabrication of such connectors is a matter of micromachining and is quite time consuming and out of the research area of this thesis. What's more, a rigid connector lowers the integration and miniaturization level of our proposed foil significantly. There is no use of making everything thin and flexible if a bulky connector is attached to it later on. This section describes the effort to embed and connect bare fibers into the foil. A standard multimode fiber diameter that we can use is 125 μm . This is in the same thickness range as the optical foil, so it does not degrade the compactness of the foil. If using a plastic optical fiber (POF) instead of a glass fiber, the flexibility of the foil can be continued along the fiber.

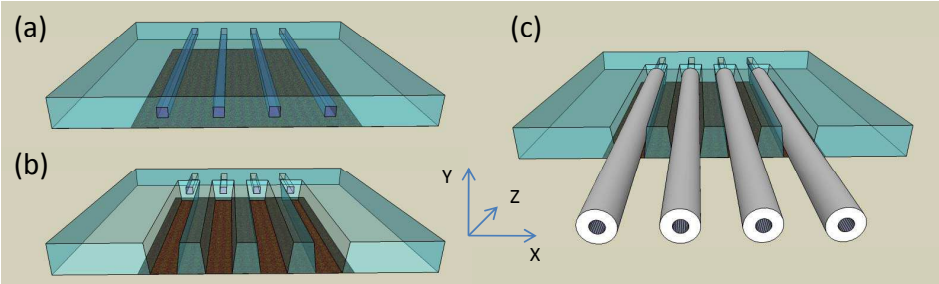

Figure 7.32: 3D schematic of the process flow to embed 125 μm diameter optical fibers inside the optical waveguide foil.

Figure 7.32 shows a 3D schematic of the process flow to embed 125 μm diameter optical fibers inside the optical waveguide foil. At the fiber embedding location, we provide a sputtered 1 μm thin copper layer (Fig.7.32(a)). This happens in the same process step and at the same Z-level as the metallization of the micro-via's and fan-out of the embedded opto-electronics. U-grooves are laser ablated at the axes of the waveguides (Fig.7.32(b)) and the fibers are simply glued into the U-grooves with transparent glue (Fig.7.32(c)). Pictures of the copper island underneath the waveguides are shown in Figure 7.33.

Figure 7.34 shows the laser ablated U-grooves as an extension of the waveguides and using the copper layer underneath as laser stop. The grooves are ablated dynamically (moving the sample table while ablating). Dynamical ablation results in a disuniform groove-depth at the beginning and the end of the groove. This is easily overcome by an additional laser step which ablates these groove-ends down to the copper island level.

In this same step, the end facet to the waveguides is ablated (see Fig.7.34(left)). Optimizing the laser parameters results in a well reproducible groove-width. Ta-

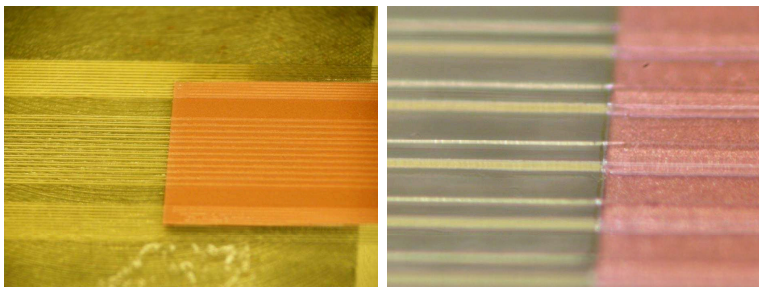

Figure 7.33: Copper island underneath the waveguides stack as laser stop for the U-grooves for optical fiber embedding.

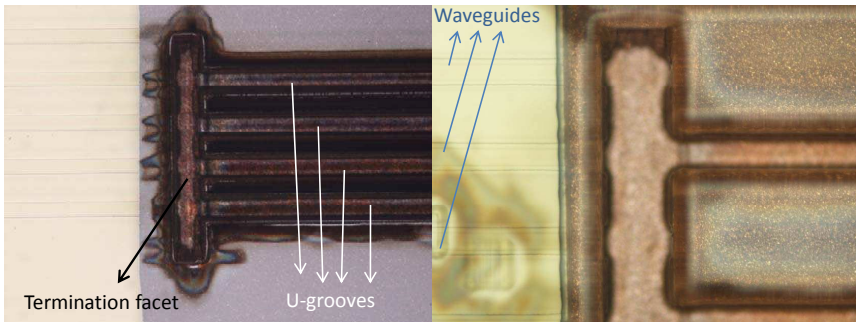

Figure 7.34: Laser ablated U-grooves for the embedding of optical fibers inside the optical foil.

ble 7.2 shows these parameters. One groove actually exists of two grooves overlapping each other with a groove-to-groove distance of 25 μm . In other words: if you ablate a groove according to Table 7.2, it will be 25 μm too narrow, so you move the sample table for 25 μm and ablate again.

Table 7.2: Excimer laser ablation parameters for the fabrication of U-grooves for the embedding of optical fibers inside the optical foil.

Excimer laser U-groove parameters	
Laser parameter	Parameter value
Puls Energy	10 mJ
Projection mask	1000 x 1000 μm ^{2}
Translation speed	100 μm /s
Puls repetition frequency	140 Hz
Fluence	214 mJ/cm^2
# repetitions	4

When ablating the grooves, it is important that the flex sample is already released from the temporary glass carrier, since the stress inside the Truemode™ Backplane Polymer would be too high. Any irregularities in the build-up, like these U-grooves can cause a crack in the substrate.

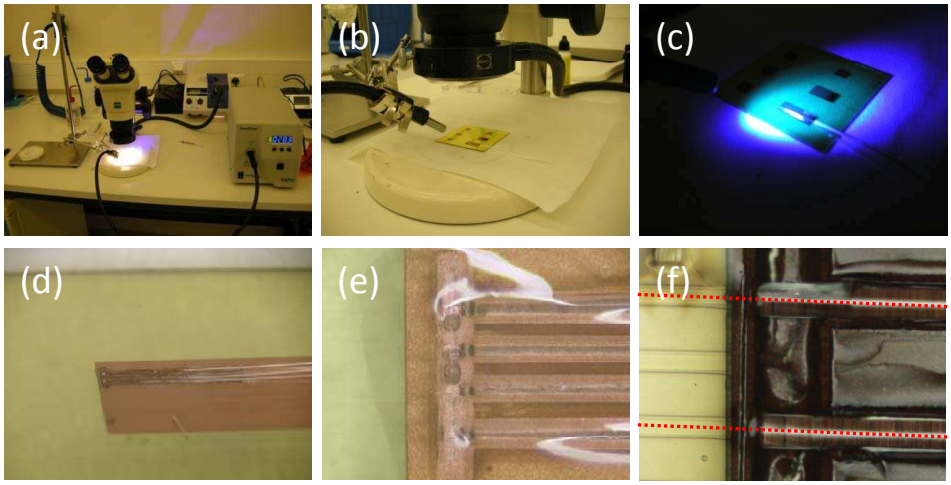

Figure 7.35: Mounting of the optical fibers inside the laser ablated U-grooves (a, b & c), side view of the mounted fibers (d) and top view (e & f).

The gluing of the fibers inside the grooves is done manually. While pressing the fibers down in the grooves with a small glass plate, an UV lamp is positioned above the sample to cure the UV curable glue. Figure 7.35(a) & (b) shows pictures of this mounting step. Fig. 7.35(c) shows the UV exposure of the sample. The mounted fibers are shown sideways in Fig. 7.35(d) and from the top view in Fig. 7.35(e) & (f). In the latter, it is clearly visible that the fiber cores are positioned at the same axis as the waveguides.

The alignment of the optical fiber cores with respect to the polymer waveguide cores is determing for the coupling loss of the proposed interconnection system. The X, Y and Z orientation that we will use in this discussion are shown in Figure 7.32. The Y alignment of the fibers is determined by the thickness of the polymer layers between the copper laser stop and the waveguides. This is mainly a $\pm$ 7 μm thick Truemode™ Backplane Polymer isolation layer (see Section 7.5) and the waveguide undercladding layer of $\pm$ 30 μm . The variation in the thickness of these layers is described in Chapter 3, Section 3.3.2 and is about 5 μm. The variation of the fiber mounting glue thickness underneath the fiber also contributes to the Y-direction alignment accuracy, but this is expected to have a small impact of only 1 or 2 μm , since the fiber can be firmly pressed down during the

curing of the glue. The positioning in the X-direction depends on the width of the U-groove, which can be controlled with a few microns accuracy. The Z-direction positioning is less critical and can be very accurate by pushing the fiber against the waveguide facet.

Figure 7.36 shows a completed optical waveguide foil connected to two optical fibers, bended in different directions and a close-up of the connection (right).

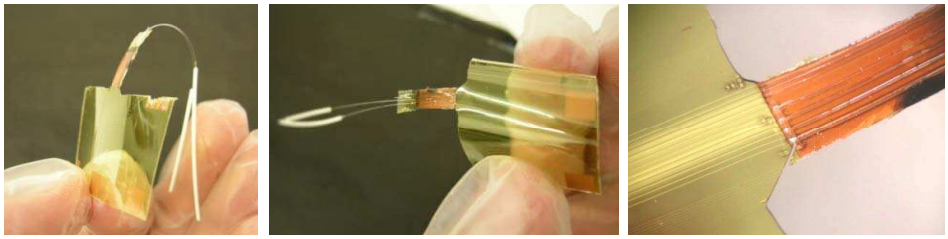

Figure 7.36: A completed optical waveguide foil connected to two optical fibers, bended in different directions (left and center) and a close-up of the fiber-connection (right).

7.7 Conclusions

The vertical optical functionality of VCSEL's and Photodiodes introduces the need for out-of-plane coupling towards the horizontal waveguides. The use of laser ablated micro-mirrors and pluggable mirror inserts has been investigated in detail in [1]. This chapter investigated the compatibility of these two coupling approaches with the embedding technologies developed in Chapter 6. The main differences with the research in [1] are the presence of an embedded chip underneath the waveguides, the use of another waveguide patterning technology and other waveguide material.

Ray tracing ZEMAX simulations were performed on the embedded optical link build-up. Main dimensional contributors to the total optical loss of the system showed to be the Z-misalignment of the micro-mirrors and the mirror angle variations. Comparison of the laser ablated mirror and the mirror plug showed that the total optical loss and the variation on this loss is significantly lower for the mirror plug. Simulations on the waveguide dimensions showed that the 50 x 50 μm ^{2} cross-sectional size - chosen for its compatibility with optical fiber core sizes - is the most profitable.

Micro-mirrors using laser ablation can be fabricated in two different ways. One way is to tilt the laser optics in such a way that the laser beam incidents the sam-

ple surface under an angle, creating a 45 degree tilted trench. The other way is the distributed laser ablation using a triangular beam shape. Characterization of the fabricated mirrors pointed out three major drawbacks. The depth of the laser ablated trench could not be well controlled, which is absolutely necessary since a chip is embedded underneath the waveguides. The core and cladding material of Truemode™ Backplane Polymer have a very different taper angle, resulting in an irregular non-flat mirror shape due to the interface of core and cladding. Moreover the positioning of the micro-mirror is dependent on the uppercladding thickness on top the waveguide, which have proven to vary with ± 10 μm .

A process for the fabrication of pluggable micro-mirrors was presented using a 45 degree polishing approach. A piece of a 500 μm thick Polyimide wafer was clamped in a 45 degree trench and polished down to a mirror surface Ra roughness of 13.5 nm (measured on a 50 x 50 μm ^{2} area). Consecutively, the polished PI motherpiece is lapped to a final thickness of 100 μm and lasercut into many single mirror plugs. This process allows the mirror facet angle to be within a $\pm$ 1 degree window, with a coupling efficiency of about 90%. Alternative fabrication methods like Wire-EDM and Deep Proton Writing (DPW) were also investigated.

The mirror plug components were integrated and aligned with 10 μm accuracy inside the layer build-up to couple the light from the waveguides to the opto-electronics. Finally, optical communication from and towards the foil with optical fibers was made possible by embedding and aligning single bare optical fibers inside the foil, eliminating the need for a bulky, rigid connector unit.

References

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Chapter 8

Characterization of the embedded optical link

This PhD thesis presents the realization of a flexible optical waveguide foil with embedded ultra thin opto-electronics, metallization and coupling elements. Every process step, optimization and consideration during this research is described in earlier chapters. This chapter focuses on the characterization of the complete system, consisting of the optical power budget, optical crosstalk, high-frequency behavior, mechanical flexibility, reliability and heat management.

8.1 Introduction

The realization of the embedded optical flexible link presented in Chapter 6 and Chapter 7 can be seen as a new technology platform for flexible opto-electronics. While optical on-board interconnections are becoming a well known alternative for electrical interconnections on board, it is still missing compactness. The flexible optical link presented here reaches the highest degree of miniaturization in this field to our knowledge. Together with the miniaturization, the embedded optical link also introduces flexibility. Flexible waveguides have proven their usefulness in the market today as an optical wiring method, but complete flexibility of the system was never contemplated. Because of the uniqueness of this technology and its possible applications so far, it is not straightforward to compare its performance with todays of-the-shelf technologies. No standard requirements or testing methods are established yet in this field of technology. In this chapter, we try however to characterize different aspects of the system using measurement techniques used for rigid opto-electronics and for electronics. The optical power budget will be analyzed to map the different contributors to the optical losses

over the complete link. Furthermore, optical cross-talk, mechanical flexibility, high-frequency behavior, reliability and heat management will be investigated.

8.2 Optical power budget

When driving current through the VCSEL in the embedded optical link, it will emit a certain amount of optical power inside the flexible optical foil, at least when the driving current is above the threshold value. With the use of optical coupling elements and light confining waveguides, we try to guide as much power of the light towards the photodiode, 2 cm further at the end of the optical link. Without any optical loss, all of the power would arrive at the photodiode, but in reality, a significant part of the optical power will be lost due to coupling loss, absorption, divergence, misalignments, scattering, reflections, etc.

8.2.1 LI curves of the opto-electronic components

We could use the values given in the data sheet of the VCSEL/PD to calculate the optical power emitted and detected (given the electrical currents), but we rather use the actual measured optical power.

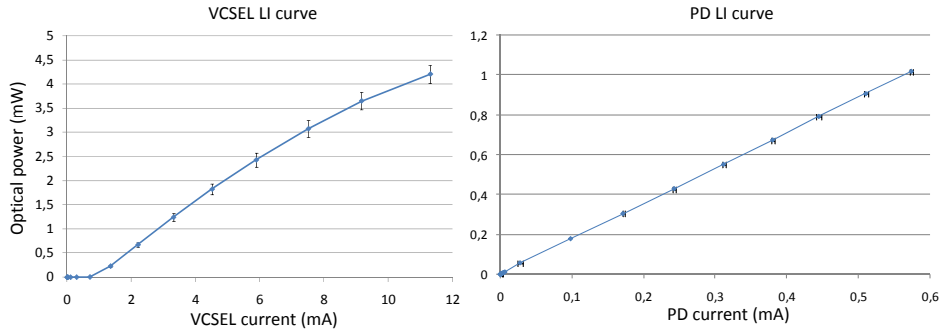

Figure 8.1: LI curve of an ULM Photonics 850 nm VCSEL ULM850-05-TT-C0104U (left) and a AlbisOptoelectronics photodiode PDCA04-70-GS (right).

Figure 8.1(left) shows the optical power of a VCSEL (ULM Photonics ULM850-05-TT-C0104U, see Chapter 5, Table 5.6 for the specs) versus the driver current and standard deviation, measured by aligning a 62.5 μm core optical fiber (coupled to power meter) above the active area of the VCSEL. Figure 8.1(right) shows the current through a photodiode (AlbisOptoelectronics PDCA04-70-GS, see Chapter 5, Table 5.6 for the specs) due to the incident light from an aligned 50 μm core optical fiber (coupled to a 850 nm laser source) above the active area of the pho-

todiode. With this information, we can quite accurately calculate the total optical link loss starting from the measured VCSEL and PD LI curve.

8.2.2 Optical loss breakdown

A CCD camera is very useful to get a visual picture of the location of optical losses in the optical link. Figure 8.2 shows CCD camera screenshots above the VCSEL and the PD for different voltages over the VCSEL. The difference in optical loss distribution when applying tilted laser ablated micro-mirrors and embedded mirror plugs in clearly visible.

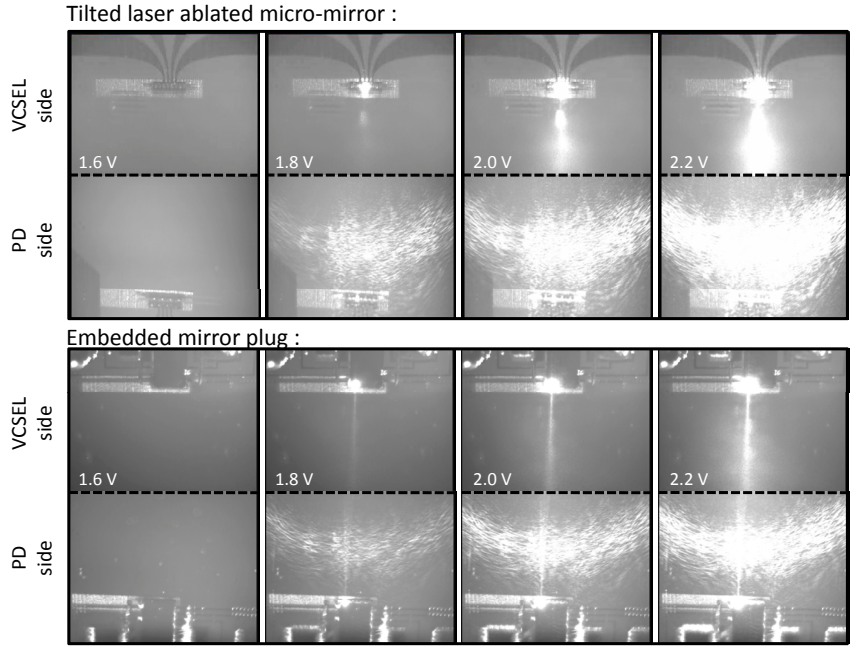

Figure 8.2: CCD camera screenshots above VCSEL and PD for an embedded link with laser ablated micro-mirrors (top) and with embedded mirror plugs (bottom).

We can see that the light is much better coupled in the waveguide when using mirror plugs. At the VCSEL side for laser ablated mirrors, we see a lot of light being coupled upwards out of the sample, instead of inside the waveguide. Figure 8.3 shows the optical power which can be detected above the VCSEL (for laser ablated mirrors and for embedded mirror plugs) by mounting an optical power meter on top of the embedded link, like depicted in the schematic cross-section on the right. The optical power detector has a circular active area of 10 mm diam-

eter. For the laser ablated mirrors, we measure a significant power loss of 3.68 dB, which means that half of the VCSEL emitted light has already disappeared from the optical link right at the beginning. This could be the result from the non-flatness of the laser ablated micro-mirror surface or the mirror Z-misalignment (see Chapter 7, Section 7.3).

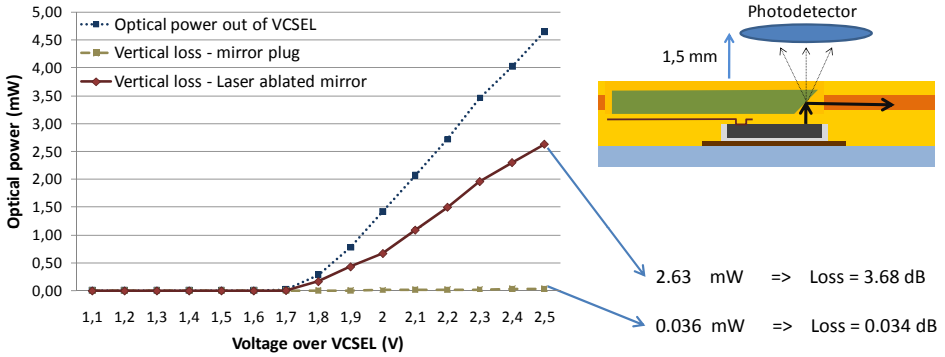

Figure 8.3: Optical power detected right above the VCSEL inside the optical link for laser ablated mirrors and mirror plug inserts.

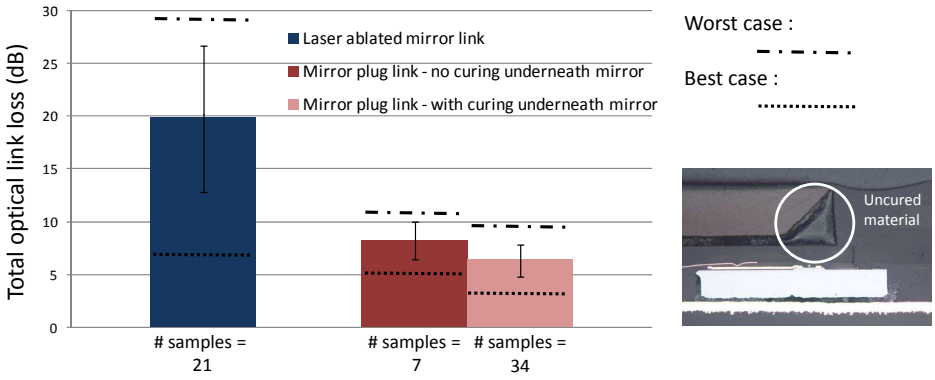

Figure 8.4: Average, standard deviation, worst case and best case of the total optical link loss for different coupling mirror situations.

The total optical power loss inside the link is subject to many variations in misalignments and layer thicknesses, resulting in a variation of the total optical loss. Therefore it is useful to measure the total optical link loss for as many samples as possible and calculate the average and the standard deviation. Also the best and worst case is interesting to get an idea of the reproducibility of the fabrication process. To measure the total optical loss, we drive a controlled current through the

VCSEL and measure the current through the photodiode. We use the information from the measured LI curves of the VCSEL and PD to calculate the conversions from electrical to optical power and vice versa.

Figure 8.4 shows all this information for embedded links with laser ablated mirrors and with mirror plugs without/with curing of the volume underneath the mirror facet. The average link loss is 19.8, 8.2 and 6.4 dB respectively. We can conclude that the uncured area underneath the mirror facet causes an additional 0.8 dB per mirror plug. Of course this curing problem can be solved by tilted UV-exposure like explained in Chapter 7, Section 7.5. The difference in optical loss between laser ablated mirrors and mirror plugs is significant. The best case when using laser ablated mirrors is worse than the average when using mirror plugs. The large variation in loss for laser ablated mirrors can be found in the large variations in alignment and angle of the mirrors (see Chapter 7, Section 7.3).

The light is coupled two times over 90 degrees, once at the VCSEL side and once at the PD side. To define which share each side has in their contribution to the total optical link loss, we sawed the 2 cm long waveguide link into two parts of 1 cm (Figure 8.5(a)). The end facets of the waveguides were polished to minimize their roughness. Consecutively we measured the two optical half link losses as depicted in Figure 8.5(b) & (c). For the VCSEL side, a 62.5 μm core size optical fiber (coupled to optical power meter) was aligned with the waveguide facet, while the VCSEL was current driven. For the PD side, a 50 μm core fiber (coupled to a 845 nm laser diode source) was aligned with the waveguide facet, while the PD current was measured.

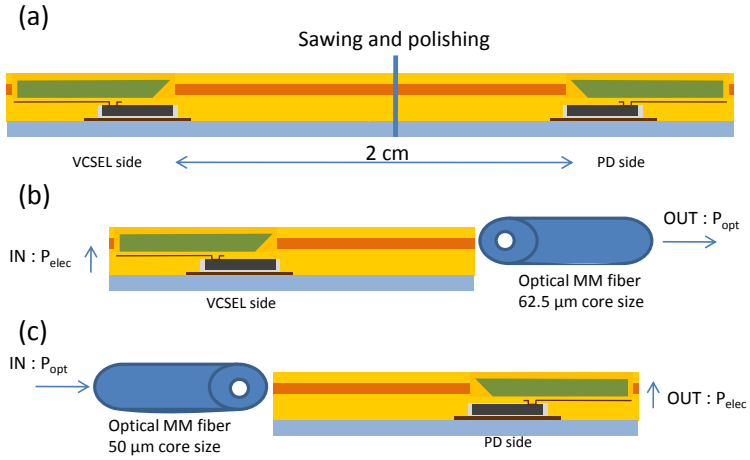

Figure 8.5: Set-up for the optical loss measurement of both halfs of the embedded optical link.

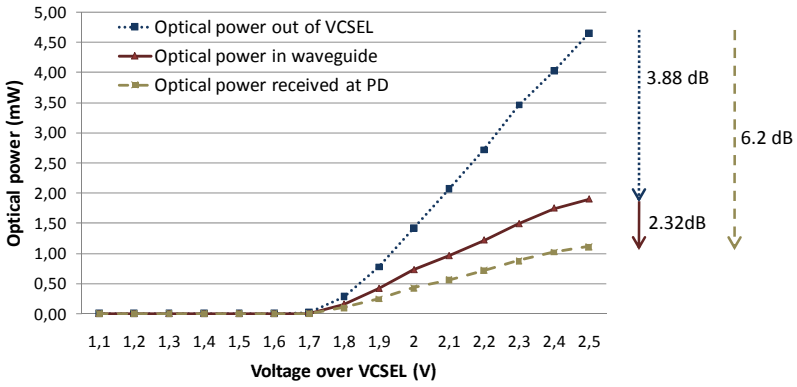

Figure 8.6: Results from the optical power loss measurement of both halfs of the embedded optical link.

The measurements are shown in Figure 8.6. The blue curve represents the optical power coming out the VCSEL. The red curve is the power measured at the end of the waveguide from the VCSEL side. The green curve is the power measured at the photodiode, if the power of the red curve is emitted with the laser diode source inside the start facet of the waveguide at the PD side. Halfway the embedded optical link, we see that about 3.9 dB of the optical power is lost and an additional 2.3 dB in the second half. This matches with the simulations in Chapter 7, Section 7.2, which predicted that most of optical power loss can be found at the VCSEL side.

8.2.3 Mirror facet metallization

When using laser ablated mirrors, we have two options. If we do not metalize the mirror facets, the mirrors will act as total internal reflection (TIR) mirror due to the large difference in refractive index between Truemode™ Backplane Polymer and air. If we metalize the mirrors they will act as reflecting mirrors. It is difficult to predict which approach is the best. It is however very easy to experimentally determine this. We measured the total optical link loss for samples with laser ablated mirrors before and after metallization. The results are shown in Figure 8.7. From the measurements, we can conclude that the metallization of mirrors results in a $\pm$ 1.4 dB extra loss per mirror. In another PhD work [1] at CMST Microsystems, the same detrimental effect of metallization on the coupling efficiency was observed. The cause was found in microscopic surface modifications due to the sputter metal deposition. The mirrors in this work however, are metalized using vapor deposition and no surface irregularities could be seen. Due to the poor performance of laser ablated mirrors in comparison with mirror plugs, we will

leave this question unanswered.

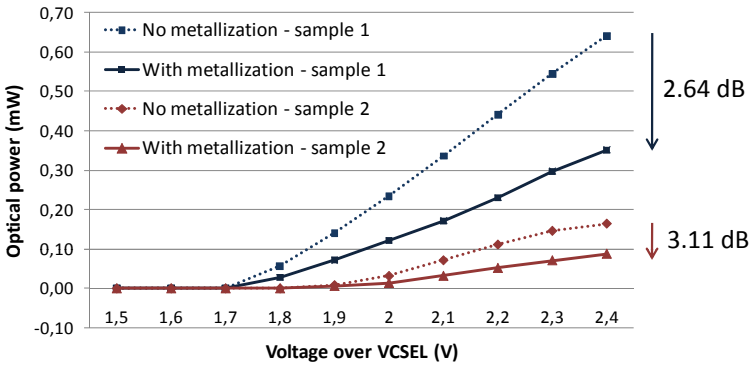

Figure 8.7: Total optical link loss with tilted laser ablated mirrors before, and after gold deposition on the mirror surface.

8.2.4 Optical crosstalk

In Figure 8.2 with the CCD camera pictures, we could see a lot of light being dispersed at the end of the waveguides. This phenomenon is not visible at the VCSEL side. Most probably, this light is coupled into the cladding layer at the VCSEL mirror coupling and manifests itself further away in the direction of the photodiode by exiting the cladding upwards. The presence of light in the cladding not only implies light being lost from the aimed optical pad, but also cross-talk to neighboring channels. Cross-talk is the phenomenon where the information on the channels is disturbed by information on neighboring channels.

Figure 8.8 shows the crosstalk in neighboring plane waveguides (left), and the crosstalk of neighboring complete optical links with embedded mirror plugs (right). The first measurement was performed by coupling light from a 50 μm core optical fiber (coupled to a 845 nm laser diode source) into one waveguide, and measure the power of the light coming out of the neighboring waveguides by aligning a 62.5 μm core optical fiber (coupled to an optical power meter). The waveguides have a pitch of 250 μm meaning that a waveguide at a distance of 250 μm is the first neighbor and the waveguide at a distance of 500 μm the second neighbor and so on. The total optical link crosstalk was measured by driving current through one VCSEL of a 1 x 4 VCSEL array and measuring the current through the other three PD's on the 1 x 4 PD array. The crosstalk to the closest neighboring link is about -17 dB. This is much higher than the crosstalk of -34dB for the planar waveguides. The difference is most probably caused by the distance between the mirror plug mirror facet and the start of the waveguide

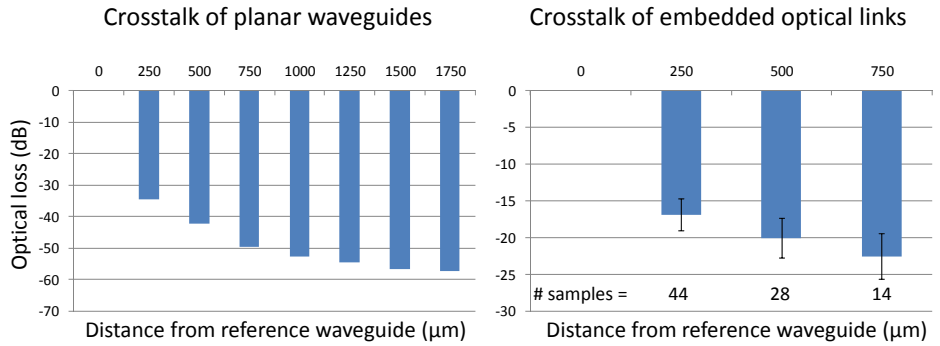

Figure 8.8: Crosstalk in neighboring plane waveguides (left) and crosstalk in neighboring complete optical links with embedded mirror plugs (right).

as explained in Chapter 7, Section 7.2. The light pad from the VCSEL to the start of the light confining waveguide is quite long. In this pad, the light is subject to divergence, resulting in light being emitted next to the waveguide, into the cladding layer. In literature, a -30 dB crosstalk is required for high performance optical data buses. We do not reach this requirement with the measured -17 dB.

8.3 High frequency behavior

To demonstrate the proof-of-principle of the embedded link, a simple lay-out with side launch coaxial SMA connectors and SMD components was assembled on a rigid FR-4 substrate for easier handling. SMD components could be placed on embedded copper tracks by removing the polymer on top these tracks by laser ablation. The same laser ablation process flow as in Chapter 6, Section 6.4.4 can be used. Figure 8.9 shows pictures of the opened contact pads in the middle of the substrate for the SMD components (Fig. 8.9(a & b)) and at the edge for the side launch coaxial SMA connectors (Fig. 8.9(c)).

Figure 8.10 shows a special design that allows us to do time and frequency domain characterization at high-speed/high-frequency using standard 50 Ohm test equipment, without requiring a VCSEL driver to drive the VCSEL's and without requiring a transimpedance amplifier for the photodiodes. At the transmit side, the bias voltage for the VCSEL's is added to the high frequency test signal by an external bias tee. Since the impedance of the (biased) VCSEL's is close to 50 Ohm, no termination resistors are needed on the board, and the VCSEL's can be driven directly by a network analyzer (e.g. to measure the analog bandwidth) or a pattern generator (e.g. to measure an eye diagram). At the receiver side, the photodiode current is converted to a voltage level by a 50 Ohm resistor to

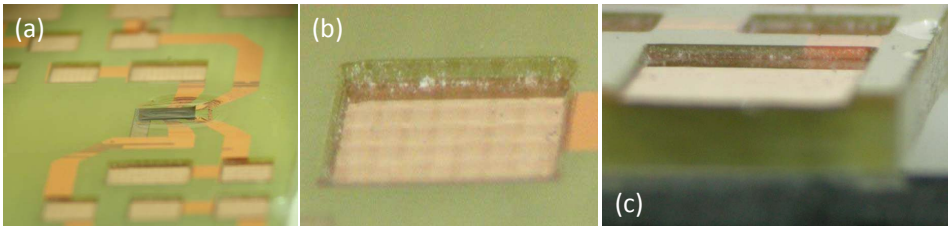

Figure 8.9: Pictures of the laser ablation opened contact pads in the middle of the substrate for SMD components (a & b) and at the edge for side launch coaxial SMA connectors (c).

ground. This 50 Ohm resistor also serves as output matching resistor so that this simple receiver can be directly connected to standard 50 Ohm test equipment. The photodiode bias voltage (connected to the cathode) is provided by a separate wire and decoupled to the ground on the board with a 10 μF capacitor.

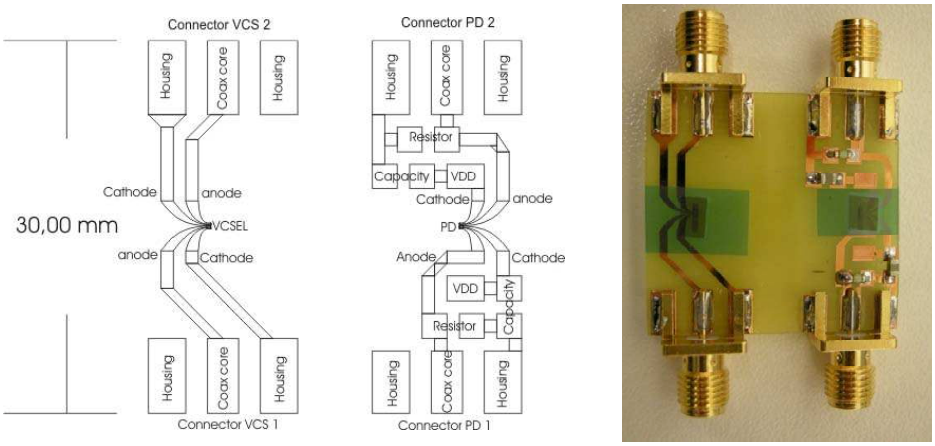

Figure 8.10: Design (left) and assembled rigid sample (right) for the embedded optical link to do time and frequency domain characterization at high-speed/high-frequency.

The assembly of the sample consists of the soldering of the SMD and SMA components to the opened contact pads. This should be done at a solder temperature of 250 ^{o}C. Soldering at higher temperatures leads to local deforming of the surrounding Truemode^{TM} Backplane Polymer material and contact pad destruction. To clamp the SMA side launch coaxial connectors, we have to thin down the substrate from the back to fit the connectors and allow the attachment to the substrate to be strong. Figure 8.11 shows the soldering of the SMD and SMA components onto the opened contact pads (Fig. 8.11(a & b)) and the side view on the thinned substrate (Fig. 8.11(c)).

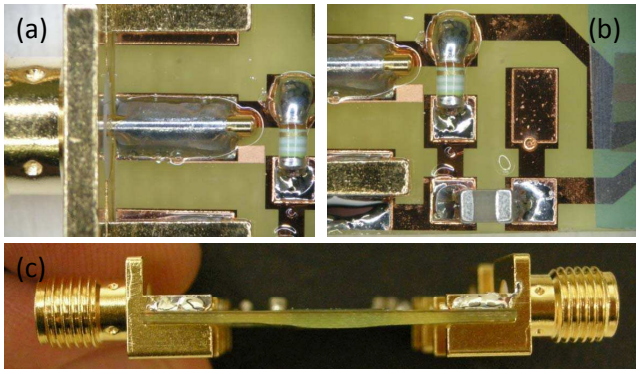

Figure 8.11: Soldering of the SMD and SMA components onto the opened contact pads (a & b) and a side view on the thinned substrate (c).

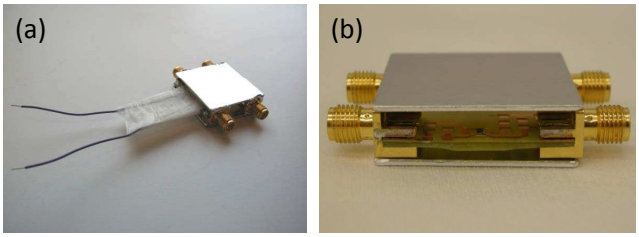

Figure 8.12: Soldered grounding/shielding plates and PD bias voltage wires to the rigid embedded optical link.

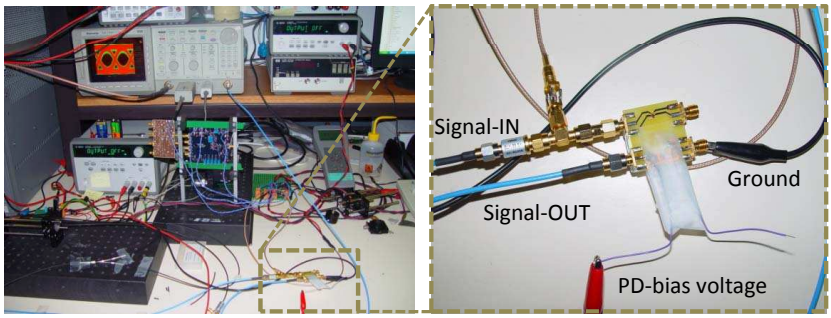

Figure 8.13: Set-up used to connect the optical link to a pattern generator to generate an eye diagram (left) and a close-up on the wired sample (right).

To shield the sample from possible distortion signals, we soldered an Aluminum plate at both side sides of the sample (see Figure 8.12). These plates also function as the ground plate for all SMA connectors.

Figure 8.13 shows the set-up used to connect the optical link to a pattern generator to generate an eye diagram (left) and a close-up on the wired sample (right).

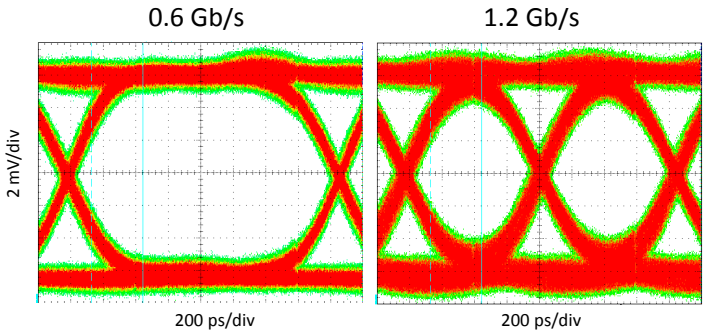

Figure 8.14: Eye diagram for 0.6 and 1.2 Gb/s for the embedded active optical link.

The eye diagram measured with this setup is shown in Figure 8.14. A very clean eye at 0.6 and 1.2 Gb/s is obtained, showing excellent operation of the optical link and the associated opto-electronic and electro-optic converters, including the high frequency interconnects and circuits required for the characterization.

8.4 Mechanical behavior

Every component in the embedded optical link is fabricated or manipulated to be ultra thin and mechanically bendable. We can now wonder how the completed opto-electronic foil acts when bended. We separate the mechanical flexibility study for three build-ups: the optical waveguide foil without embedded actives, the opto-electronic foil without the flexible waveguide and the complete stack of embedded actives + waveguides.

The first structure is the flexible optical waveguide foil. The mechanical behavior was studied in detail in Chapter 4 Section 4.7.2. The foil could be bended around 2.5 mm radius cylinders without showing any visible defect. The optical propagation loss measurements pointed out that an additional loss after 1000 times bending was 1 dB on a waveguide of 8 cm long. Bending 1000 times around 4.5 radius cylinders does not cause any additional loss.

The second structure is the same as the embedded active optical link foil but without the waveguide layers. In other words, we stop the process flow after the embedding and metallization of the embedded opto-electronics. Instead of fabricating the waveguides on top, we apply the top PI layer. This way we have a $\pm$ 50 μm thin flexible SU-8 package for opto-electronic components without waveguides or optical coupling structures. The reason to study this structure is to look at the behavior of the embedded VCSEL and its metallization features when bending to a small radius. Figure 8.15 shows the VCSEL and PD package (inside one sample) rolled up around a cylinder with a 2 mm radius in both directions (a & b). The electrical VI curve was monitored during bending by soldering thin wires to the contact pads. No changes were observed in the VI characteristics. 1000 Bending cycles in between two such 2 mm radius cylinders (Bending set-up: see Chapter 4, Section 4.7.2), does not result in any degradation of the galvanic interconnection or the embedded actives. Figure 8.15(c) & (d) shows close-ups of a 1 x 4 VCSEL array bended at a 2 mm bending radius. As can be seen on the pictures, the VCSEL array is actually bending with the substrate.

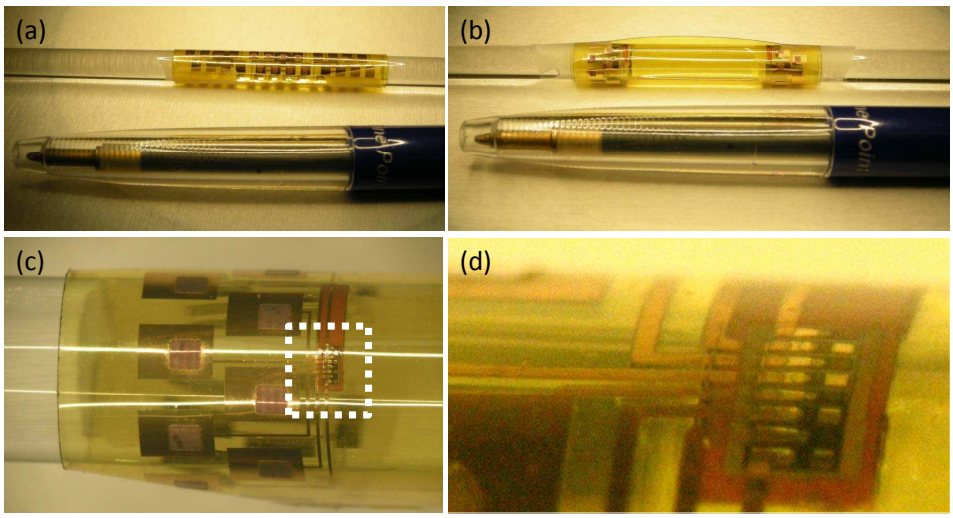

Figure 8.15: VCSEL and PD array package (inside one sample) rolled up around a cylinder with a 2 mm radius in both directions (a & b) and close-ups on the 1 x 4 VCSEL array (c & d).

The third structure is the build-up as presented in Chapter 6 and Chapter 7, being the total active optical link build-up with embedded actives, metallization, coupling structures and waveguides. As explained in Chapter 2, the waveguide materials are not really flexible. The sandwich with PI layers improved the flexibility as proved with the first structure discussed above, but the total stack of actives embedded in SU-8 and the waveguides in Truemode™ Backplane Polymer lacks

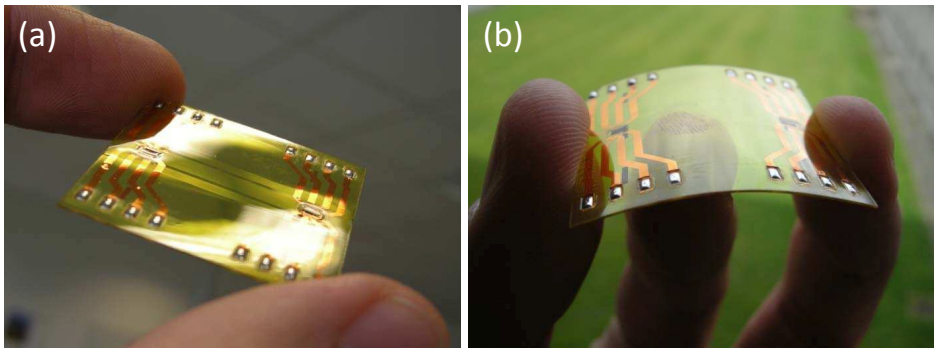

Figure 8.16: Finalized flexible active optical link substrate flat (a) and bended (b).

of flexibility. Figure 8.16 shows a finalized flexible optical link substrate with soldered contact pads and the embedded waveguides clearly visible (a). Figure 8.16 (b) shows this substrate being bended with a bending radius of about 5 cm. Further bending would probably result in breakage of the substrate. The flexibility is not satisfying with the used polymer build-up. The use of more flexible layers should solve this drawback, but commercial availability is an issue (see Chapter 2). Optimization of the layer thicknesses within the stack could also reduce the total thickness and improve the flexibility. For example, the cladding layers have an important share in the total substrate thickness. Their thickness could be reduced from 50 μm to 30 μm or even to 20 μm , reducing the total stack thickness with 60 μm . Also chip covering layer and isolation layer could be made thinner.

8.5 Reliability

A very important issue in electronics and thus also in opto-electronics and any combination of the both, is the reliability of the system. Even if a system functions perfectly after fabrication, it could malfunction after a certain time of utilization due to aging processes. The aging of electronics is mostly induced by continuously environmental temperature changes and the presence of moisture in the environment. Temperature changes imply stresses due to CTE difference between the different elements of the system. These periodical variation in stress can cause aging and thus defects into metal, semiconductor and polymer layers and components. Also humidity can slowly penetrate the system, causing oxidation of galvanic interconnects and swelling of polymer material, resulting in again stresses and - in the end - defects. The theoretical simulation of failure mechanisms is very difficult and in a complex system probably never correct. The best way to approximate the probable life time of a system is to put it through ac-

celerated aging tests. We will apply an accelerated temperature-humidity aging test (85/85 test) and a thermal cycling test to the embedded optical link.

8.5.1 Temperature cycling

Temperature cycling tests were performed on both flexible and rigid embedded optical links. The rigid links were fabricated on top of a standard FR-4 PCB board. Four of them were fabricated in Truemode™ Backplane Polymer material and three in Epocore / Epoclad material, the flexible samples were all fabricated in Truemode™ Backplane Polymer.

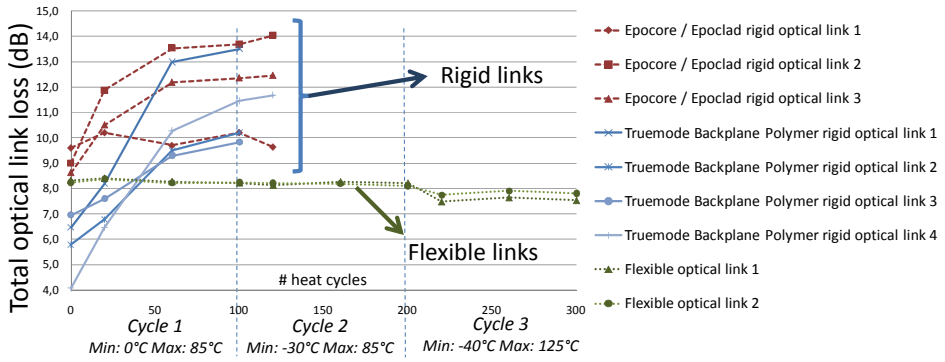

Figure 8.17: Evolution of the total optical loss of embedded flexible and rigid optical links during temperature cycling.

Figure 8.17 shows the evolution of the total optical loss of the different optical links during temperature cycling. The samples were passed through 300 temperature cycles with a different temperature profile for each 100 cycles (cycle 0-100: 0^{o}C to 85^{o}C ; Cycle 101-200: -30^{o}C to 85^{o}C and cycle 201-300: -40^{o}C to 125^{o}C). Each profile consists of a dwell of 15 minutes at both extremes and a transition speed between the two extremes of 3^{o}C per minute. A clear deterioration of the rigid links can be seen and even a total failure at temperature cycles down to -30^{o}C. The optical layers are showing cracks and delamination from the FR-4 substrate, probably caused by the CTE mismatch between the FR-4 ($\leq$ 20 ppm/K) and the SU-8 (50 ppm/K). The flexible links show no change in optical transmission due to the cycling, even up to temperature ranges of - 40^{o}C to 125^{o}C. We can conclude that the mechanical flexibility of the embedded optical links can increase the reliability significantly.

8.5.2 Humidity storage

The humidity storage 85/85 test is performed in an environment with a constant 85% relative humidity at a constant temperature of 85^{o}C. Figure 8.18 shows the evolution of the average total optical link loss during the humidity exposure. The flexible links resist the humidity much better as can be seen in the graphs. Probably the top PI layer - which was applied on the flexible links and not on the rigid links (no need for support layers) - acts as a moisture barrier for the optical layers.

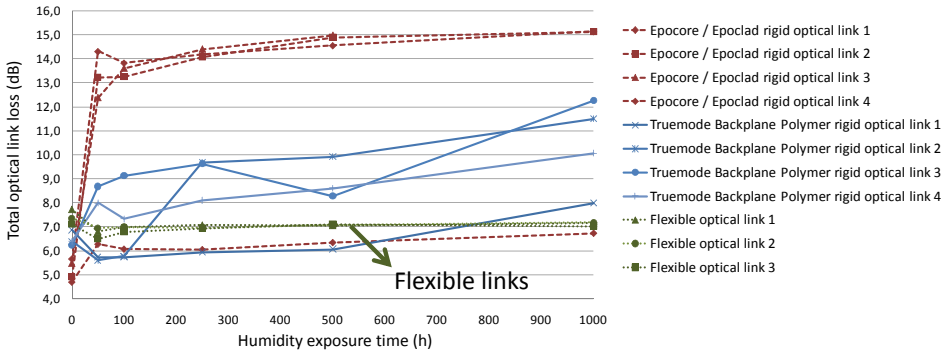

Figure 8.18: Evolution of the total optical link loss during the humidity exposure for flexible and rigid embedded optical links.

In an effort to try to separate the galvanic interconnection aging and the aging of the optical features of the embedded optical link, we did the same aging tests on an embedded IC as presented in Chapter 6, Section 6.5 on a rigid FR-4 board (without waveguides, without PI layers). This would give us an idea of the deterioration of the galvanic tracks and via-interconnections without any optical aspect in the system. Figure 8.19 and Figure 8.20 show the evolution of the via-resistance and the daisy chain resistance respectively during temperature cycling.

We see a very small gradual increase of the via-resistance. The daisy chains resistance does however not show any degradation. The highest resistance contribution to the daisy chain is the galvanic interconnection on the chip, while the copper tracks and via's in a higher polymer level above the chip level have a very small contribution. This means that we can conclude that the lower level metallization is not degraded. The via's who are close the surface show a degrading resistance, while the interconnections on the chip on the contrary do not degrade. This makes us believe that the degradation is caused by moisture instead of the temperatures cycles. The temperature cycling is not done in vacuum, but in normal air with a nominal humidity, which can penetrate the polymer. Especially for higher temperatures, there is a higher swelling of the polymer and a larger chance

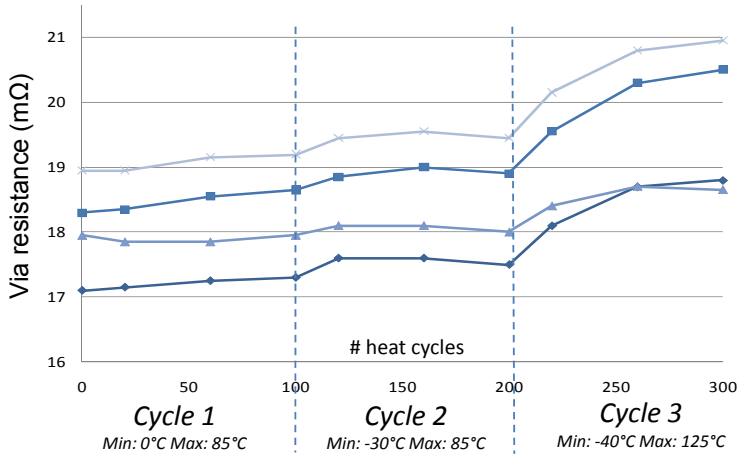

Figure 8.19: Evolution of the via-resistance during temperature cycling of an embedded IC.

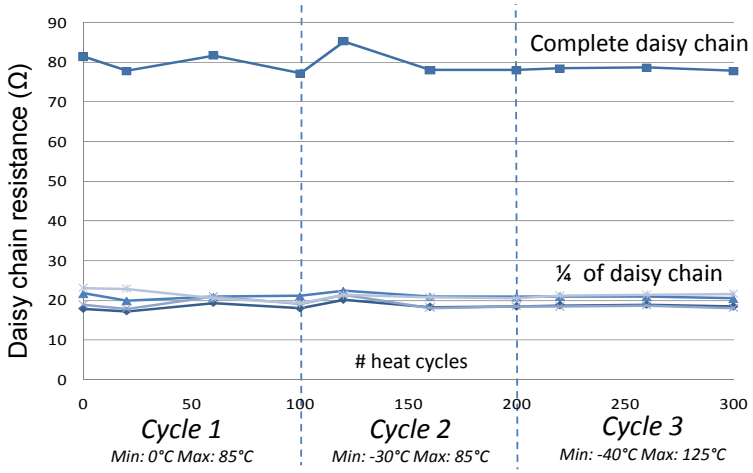

Figure 8.20: Evolution of the daisy chain resistance of an embedded IC on a rigid FR-4 board during temperature cycling.

the moisture penetrates the sample, degrading the copper tracks and via's.

To see the impact of moisture on the deterioration of embedded copper tracks and micro-via's, another embedded rigid IC sample was put through the same 85/85 humidity test as the optical links. Figure 8.21 shows the evolution of the via-resistance during the humidity exposure. After 50 hours, the average via-

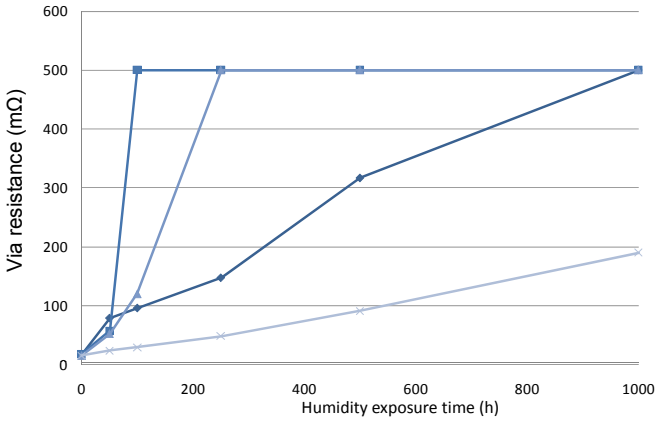

Figure 8.21: Evolution of the via-resistance of an embedded IC on a rigid FR-4 board during humidity exposure.

resistance was already 5 times higher than the initial value. After 1000 hours, every via had a resistance larger than 500 mΩ (maximum measured value). This means that our conclusion about moisture being the detrimental effect on the resistance of embedded galvanic interconnections was right. If we look at the humidity testing of the optical links however, we do not see such a fatal deterioration. In the optical link foil however, the copper tracks are more protected and isolated from the humidity in the outer world by the 150 μm thick polymer waveguide stack and 7 μm thin top PI layer. The via's are even more isolated by the PI mirror plug on top. This was not the case with the embedded IC, where the copper tracks and via's were only protected by one single 30 μm thin SU-8 layer.

A final test to confirm these conclusions is the storage of an embedded IC sample at room temperature and at nominal room humidity for 4 months. The via resistance and daisy chain resistance was measured right after fabrication and after 4 months of storage. The results are shown in Figure 8.22. Again we see a small average increase in via-resistance but no average raise in daisy chain resistance.

8.5.3 Solder reflow cycle

Soldering is a common technology for the assembly of electronic, opto-electronic components and interconnecting wires. The proposed flexible optical active foil in this PhD work is however contradictory to the assembly of bulky and these non-flexible components, since these components would have a detrimental im-

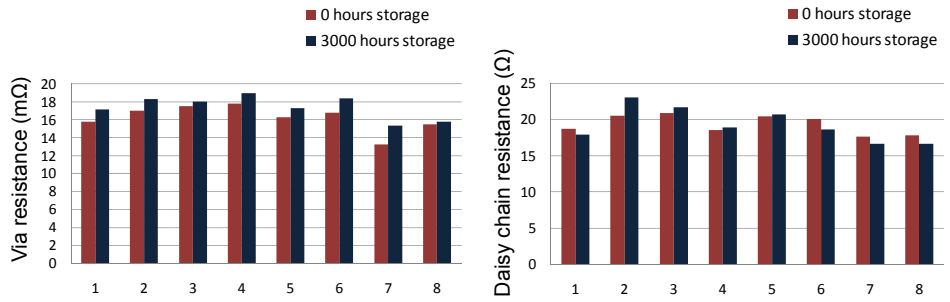

Figure 8.22: Via resistance and daisy chain resistance for an embedded IC on a rigid FR-4 board right after fabrication and after 4 months storage at room temperature and nominal room humidity.

pact on the level of miniaturization and flexibility of the system. It is however always interesting to look at the compatibility of the presented active optical foil with standard solder reflow process steps. Two flexible optical link samples were exposed to a single solder reflow temperature cycle. Figure 8.23 shows the total optical link loss before and after the solder reflow. An average additional loss of 1.3 dB was observed, a small difference but definitely no failure of the link.

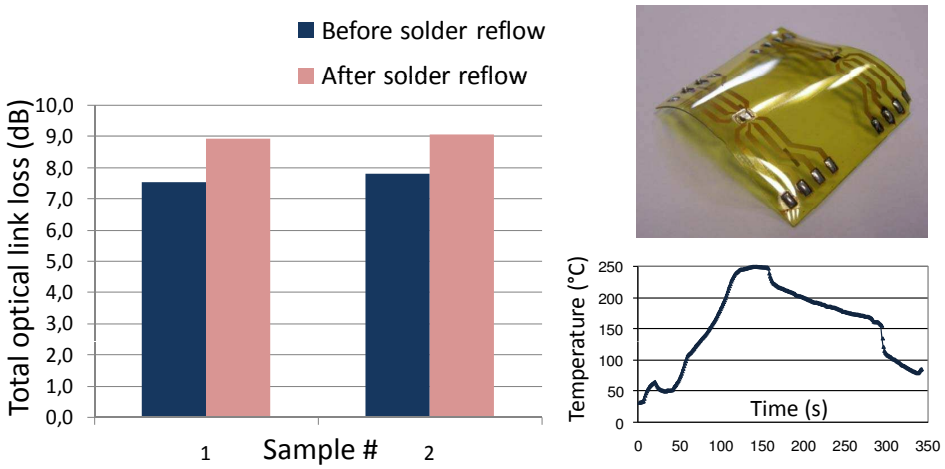

Figure 8.23: Total optical link loss changes and substrate deformation due to exposure to a standard solder reflow temperature cycle.

A picture of the sample after reflow is also included in Figure 8.23 together with a graph of the temperature profile in time. We can see that the sample is a little bit deformed. This can be explained by the fact that the sample is heated to 250^{o}C for

half a minute, which is highly above the Tg of Truemode™ Backplane Polymer of 180^{o}C. When the Tg is reached, the material changes from its glasslike state to its rubberlike state which causes changes in the materials properties. The Tg is not a measure of the materials melting point, but rather a point at which molecular bonds begin to weaken enough to cause a change in physical properties such as the dimensional stability and the flexural strength. Because of the high temperature ramp (from 50^{o}C to 250^{o}C in only 60 seconds) and the difference in CTE of the SU-8 and Truemode™ Backplane Polymer we expect high strains and stresses inside the material during warming up. Internal stresses combined with weakening of the material can result in dimensional deformations as seen on the picture. Proper mounting or lamination of the sample on or between other more stable layers or substrates would prevent this deformation to happen.

8.6 Heat management

The VCSEL's of the flexible active opto-electronic foil presented in Chapter 6 are fully embedded inside the polymer SU-8 and Truemode™ Backplane Polymer layers. In this configuration, a complete functional VCSEL array raises thermal management concerns because it is completely encapsulated with thermal insulators. Underneath the VCSEL's, a heat sink of 10 μm thick sputtered and electroplated copper was fabricated of 1.2 by 3 mm^2. Improper heat dissipation can lead to thermal runaway. The increasing temperature leads to wavelength shift, increased threshold current, reduced quantum efficiency, shortened device lifetime and higher dissipated power. Therefore, the heat management of the driving VCSEL array is a critical issue in the fully embedded optical links. The thermal management of a VCSEL-based optical module was reported in [2], the thermal resistance of a VCSEL bonded to an IC in [3] and the thermal management of an ultra thin VCSEL laminated in a PCB stack in [4]. These papers present useful information, but are not applicable to the embedded optical link. This section describes the use of two different thermal simulation methods to investigate the influence of different dimensional parameters on the heat spreading inside the embedded optical link layer build-up. This research was performed in close cooperation with the Thermo-Electronics group from the ELIS Department of the Ghent University of Professor Gilbert De Mey [5, 6].

8.6.1 Two dimensional cross-sectional model

In the two dimensional cross-sectional model, we look at the cross-section of the embedded link in the middle of the VCSEL-array. The model is invariant in the third dimension being the Z-direction as depicted in Figure 8.24. Different embedding polymers have different thermal conductivities, that is why the

Polyimide, Truemode™ Backplane Polymer and SU-8 material are all grouped together as being only one material with a thermal conductivity of 1 W/mK for the ease of the calculations. The simulated values can be easily scaled afterwards with the thermal conductivity of the used embedding material. The top and bottom edge condition is classic convection h = 10 W/m^{2}K and the edge conditions in the x-directions are adiabatic.

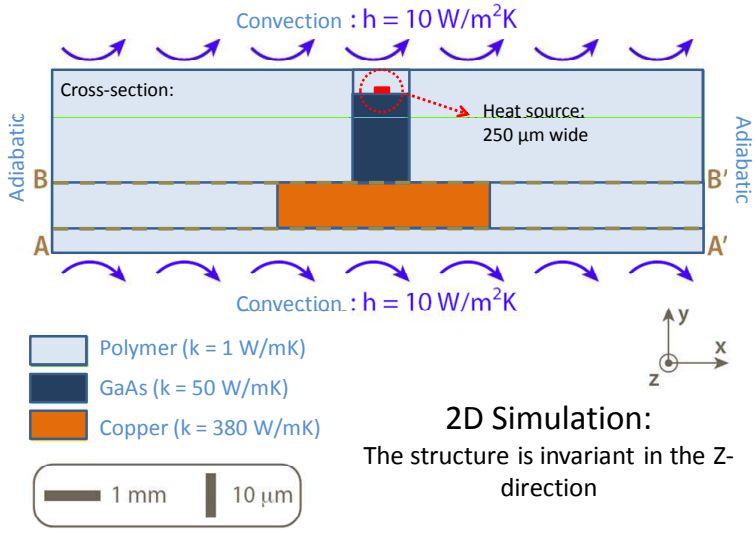

Figure 8.24: Two dimensional cross-sectional model overview.

Heat sink width

The width of the heat sink can be scaled since it is only defined by the lithography mask during the heat sink fabrication. The influence of this dimensional parameter on the heat spreading is shown in Figure 8.25(left). The normalized temperature in the source itself in function of the heat sink width in shown in Figure 8.25(right). The normalized temperature (K/mW) is the temperature above the room temperature (K) per unit of power dissipated inside VCSEL (mW). For a heat sink width of 3.8 mm, a room temperature of 20^{o}C and the VCSEL dissipating continuously 20 mW, the absolute source temperature will be 20K + (21 K/mW * 20 mW) = 440^{o}C. This is a very large temperature, which is actually a large over-estimation, since the heat can only spread in 2 dimensions instead of 3 in reality. When we do these simulations on the AA' or on the BB' axis (see Figure 8.24), there is no difference at all. As a matter of fact, the heat distributing over the complete Y-axis is completely uniform within the boundaries of the layer stack.

This can be explained by the fact that the Y-dimensions are much smaller than the X-dimensions. As a consequence, the heat can only be spread in one dimension, the X-dimension. From Figure 8.25 we can conclude that the width of the heat sink can significantly bring down the temperature of the VCSEL.

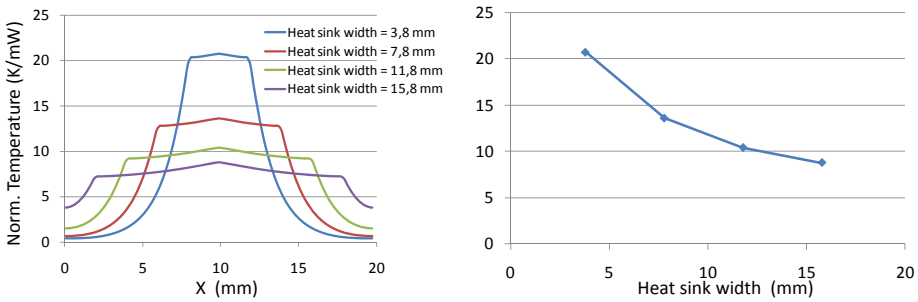

Figure 8.25: Normalized temperature distribution along the X-axis (left) and normalized VCSEL temperature (right) in function of the heat sink width.

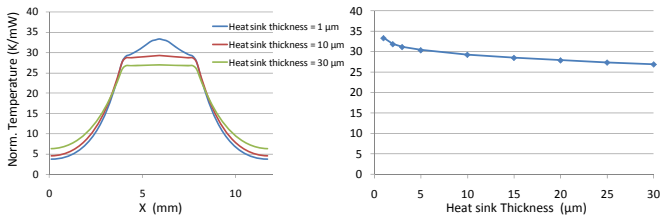

Figure 8.26: Normalized temperature distribution along the X-axis (left) and normalized VCSEL temperature (right) in function of the heat sink thickness.

Heat sink thickness

As discussed in Chapter 6, Section 6.2.1, the heat sink is fabricated by sputtering a 1 μm thick copper layer and electroplating that layer upto a thickness of 10 μm . This thickness can be varied as wished. Figure 8.26 shows the normalized temperature distribution along the X-axis (left) and normalized VCSEL temperature (right) in function of the heat sink thickness. The thickness of the copper heat sink cannot really bring the temperature of the VCSEL down, but it can be seen that the copper needs to have a minimum thickness of a few microns for a good homogenous heat spreading over the complete width of the heat sink. The 10 μm thickness is however needed to stop the laser beam when laser ablating the VCSEL cavity.

VCSEL chip thickness

The embedded VCSEL's in the embedded optical link are thinned VCSEL's of 20 μm thickness. We can however wonder which influence this thickness has on the heat spreading. Figure 8.27 shows the normalized temperature distribution along the X-axis (left) and normalized VCSEL temperature (right) in function of the VCSEL thickness. Using thinner VCSEL's results in worse heat spreading, but this effect is limited. The difference in VCSEL temperature between the original thickness of 150 μm and the ultra low thickness of 20 μm is only 22% in the normalized temperature. Actually it is not really the VCSEL thickness which causes this change in heat spreading directly. The true explanation is the fact that how thicker the VCSEL is, the thicker the total layer build-up will be, the better the heat can spread in the X-direction. This situation is a trade off. On one hand we want the foil to be as thin as possible because of flexibility and miniaturization considerations and on the other hand we want the heat spreading to be adequate.

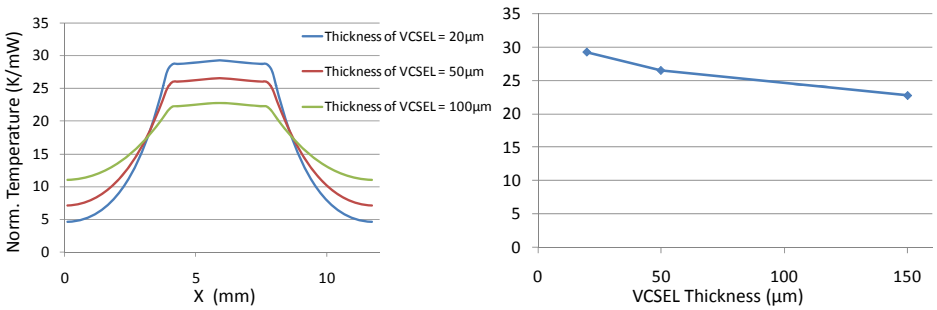

Figure 8.27: Normalized temperature distribution along the X-axis (left) and normalized VCSEL temperature (right) in function of the VCSEL thickness.

Polymer on VCSEL

In Figure 8.24, the VCSEL is covered with a 5 μm thin SU-8 layer. In the final embedded optical link, also a 10 μm isolation layer and a 130 μm thick waveguide stack will be fabricated on top of the VCSEL. This is more material which can spread the heat. Figure 8.28 shows the normalized temperature distribution along the X-axis (left) and normalized VCSEL temperature (right) in function of the polymer thickness above the VCSEL. The VCSEL normalized temperature behaves the same as for the thickness variation of the VCSEL itself. This is perfectly normal, since the principle behind it is exactly the same: the thicker the total foil, the better the heat spreading. Again, we have a trade-off situation.

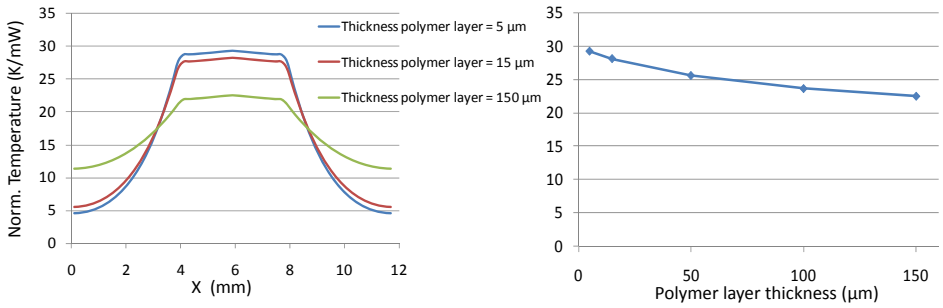

Figure 8.28: Normalized temperature distribution along the X-axis (left) and normalized VCSEL temperature (right) in function of the polymer thickness above the VCSEL.

Heat spreading management

Like demonstrated above we have to make choices for the dimensional parameters. Often the right choice for heat spreading is the wrong choice for the flexibility and compactness of the foil. Figure 8.29 shows an overview of the influence of all studied parameters on the VCSEL normalized temperature. The thickness of the VCSEL and the polymer on top of the VCSEL should be as thin as possible to improve the flexibility of the foil. The width of the heat sink is the only parameter we can scale up without losing functionality or flexibility and has fortunately a higher impact on the VCSEL temperature. This means that the best choice is to scale the heat sink dimensions in order to achieve the desired heat spreading. Figure 8.29 also shows the VCSEL temperature when the convection at the top PI layer would be absent, showing that the lack of convection at one side of the foil, would be detrimental to the heat spreading. It must be said however that this situation is almost never the case. If the foil would be laminated between other foils or between rigid boards, we would not have convection, but thermal conduction through these laminates or boards allowing the VCSEL to spread its heat in 3 dimensions, which is even better than convection cooling.

Another solution to scale the heat sink is to laser ablate the bottom PI layer away underneath the heat sink. This way the heat sink bottom surface is opened to the air. Now we can sputter and consecutively electroplate on the bottom PI layer from the back side, resulting in a heat sink, which could be theoretically as large as the foil itself (see Figure 8.30).

Using this method, all heat sinks on the substrate can be scaled with only one process step. The addition of a 10 μm thick copper layer to the foil, will not hinder the foils flexibility since copper is a very soft metal and has proven its flexibility in many other flexible electronics applications.

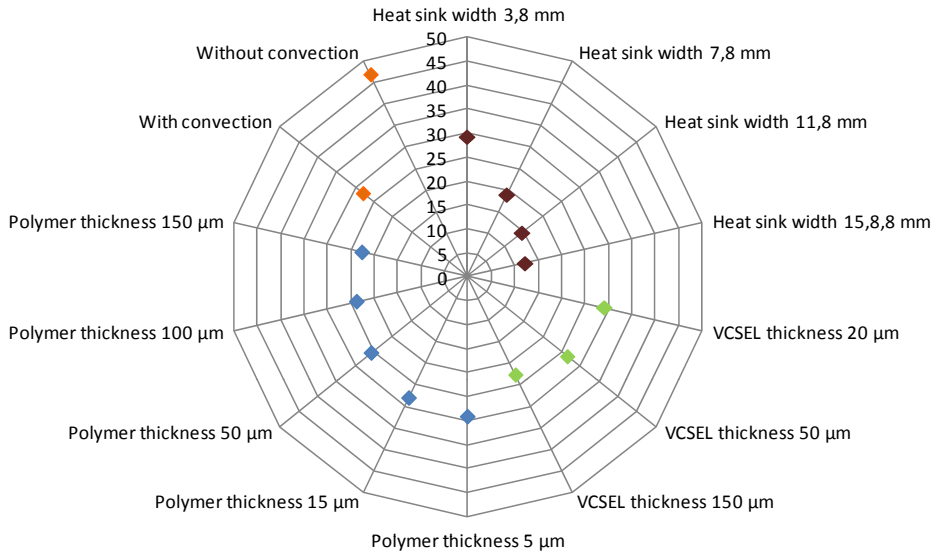

Figure 8.29: Overview of the influence of all studied parameters on the VCSEL normalized temperature.

8.6.2 Thin plate model

The two dimensional cross-sectional model revealed that the heat distribution over the thickness of the foil is uniform and that the heat spreading is only significant in the X direction. This knowledge allows us to use another thermal simulation method, which will give us a much better view on the absolute temperatures inside the foil: the thin plate model. The principle is explained in Figure 8.31.

We are no longer analyzing the cross-section but the top view on the embedded VCSEL. Of course we need to do a projection of the thermal properties of all used material to this plane. For example, when we look at the place where the VCSEL is mounted, we only see the VCSEL, but in fact, is a stack of polymer, copper, GaAs-VCSEL and again polymer. To define the right thermal conductivity for each area, we make a weighted average of the thermal conductivity of each material in that area (weighted by the thickness of each material at that location).

The heat can be spread in two dimensions using this model, which will give a good approximation of the true absolute value of the VCSEL temperature.

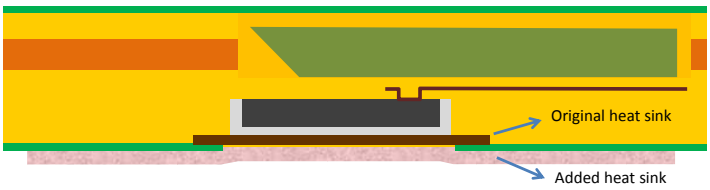

Figure 8.30: Alternative process for the scaling of the heat sink underneath the VCSEL's.

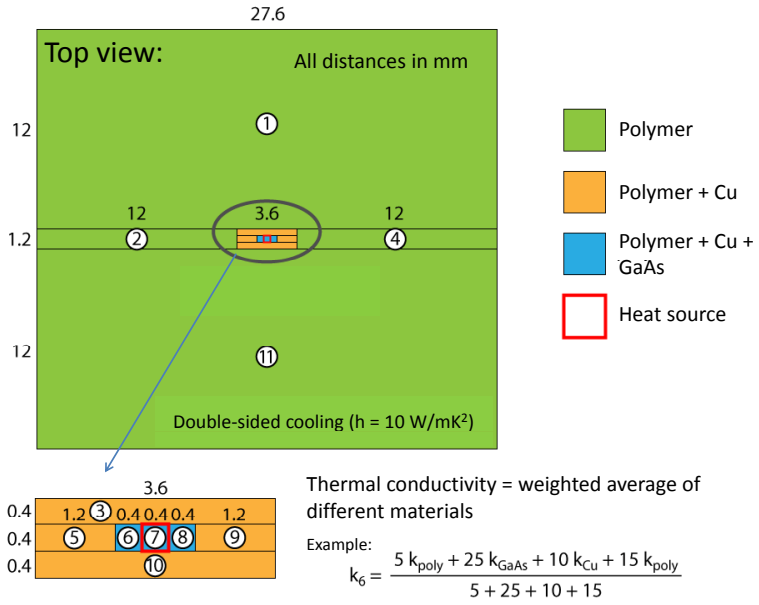

Figure 8.31: Thin plate model overview.

Heat sink dimensions

Rather than only looking at the width of the heat sink, we can now look at the 2D dimensions of the heat sink. Figure 8.32 shows the normalized VCSEL temperature in function of the heat sink length for 2 different heat sink widths (left) and the normalized VCSEL temperature in function of the heat sink total surface area (right). The copper thickness in these simulations is 10 μm . For a very small heat sink of 3 x 1.2 mm^2, the VCSEL will have a normalized temperature of 2 K/mW. The maximum driver current of the used VCSEL's is 12 mA. A voltage of 2.1 V is needed to reach this maximum driver current. This means that one VCSEL can dissipate maximum 2.1 V x 12 mA = 25.2 mW when working in continuous

mode. A 1 x 4 VCSEL array can then dissipate upto 4 x 25.2 mW = 100.4 mW. This maximum dissipated power results in a regime VCSEL temperature of [20 ^{o}C+ (2 ^{o}C/mW x 100.4 mW = 220.8 ^{o}C] when the room temperature is 20^{o}C. For a larger heat sink of 2.4 x 16 mm^2, this temperature is [20 ^{o}C+ (0.6 ^{o}C/mW x 100.4 mW = 80.2 ^{o}C]. Using larger heat sinks can reduce the VCSEL temperature significantly.

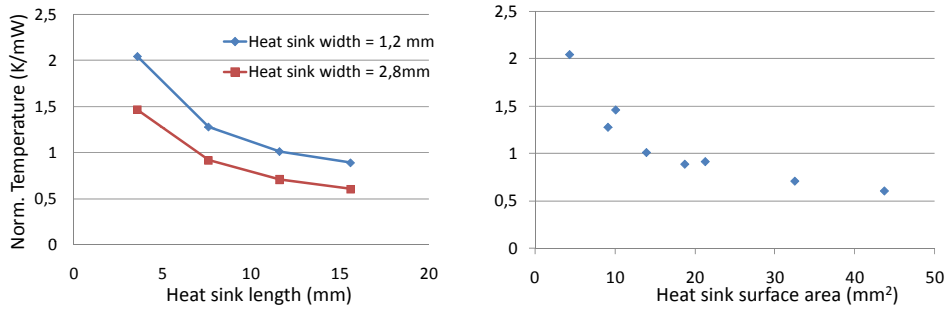

Figure 8.32: Normalized VCSEL temperature in function of the heat sink length for 2 different heat sink widths (left) and normalized VCSEL temperature in function of the heat sink total surface area (right).

Heat sink thickness

Figure 8.33 shows the normalized VCSEL temperature in function of the heat sink thickness. The heat sink dimensions in these simulations are 3 x 1.2 mm^2. The impact of the copper heat sink island thickness is similar to the impact simulated in the 2D cross-sectional model.

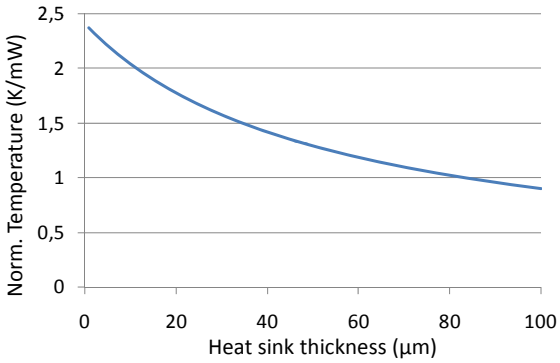

Figure 8.33: Normalized VCSEL temperature in function of the heat sink thickness.

8.7 Optical characterization of embedded VCSEL's

In Chapter 5, Section 5.5.3, we explained the optical characterization of VCSEL's and the used measurement set-up for this purpose. We discussed that every VCSEL has a slight different optical behavior and defined the mode threshold appearance of the first modes of the VCSEL as a "fingerprint" for each VCSEL.

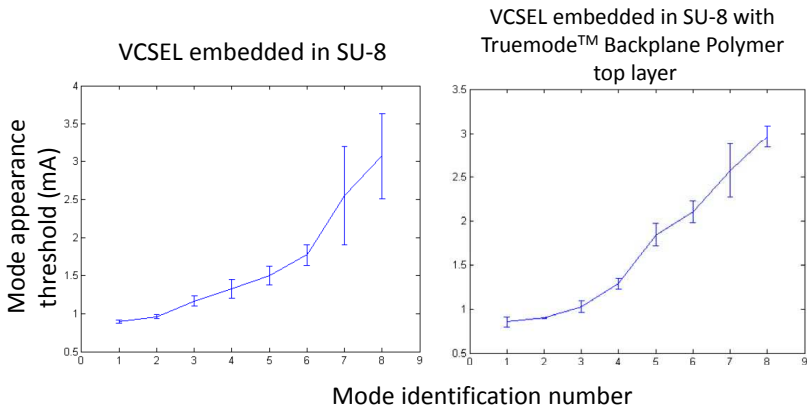

Figure 8.34: Mode appearance thresholds for embedded VCSEL's in SU-8 (left) and embedded VCSEL's in SU-8, with a 30 μm Truemode™ Backplane Polymer layer spincoated and cured on top (right).

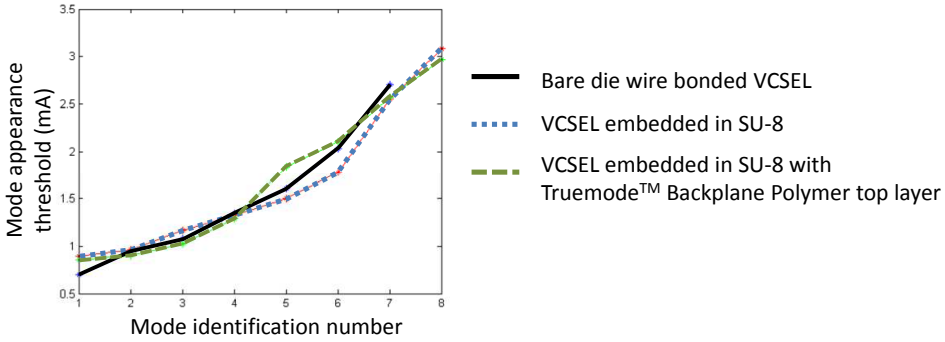

Figure 8.35: Comparison of the mode appearance thresholds for bare die wire bonded VCSEL's, embedded VCSEL's in SU-8 and embedded VCSEL's in SU-8, with a 30 μm Truemode™ Backplane Polymer layer spincoated and cured on top.

The comparison of the mode appearance threshold for unthinned and thinned VCSEL resulted in the conclusion that the thinning of the VCSEL has no influence on the optical behavior of the VCSEL. We performed the same measure-

ments with the same measurement set-up to investigate the influence of embedding on the VCSEL's optical behavior. Therefore we compare the mode appearance thresholds of a wire bonded VCSEL, an embedded VCSEL in SU-8 and an embedded VCSEL in SU-8, with a 30 μm Truemode™ Backplane Polymer layer spincoated and cured on top. Figure 8.34 shows the separate mode appearance thresholds and error bars for the latter 2 VCSEL packages, while Figure 8.35 compares the average results for the three packages in one graph. The three graphs are very close to each other, meaning that the optical behavior of bare VCSEL's and embedded VCSEL's are the same and that the optical behavior is not influenced by the embedding process.

8.8 Conclusions

This chapter handles the characterization of the embedded optical link foil as a total system. The optical power budget, optical crosstalk, mechanical flexibility, high-frequency behavior, reliability and heat management were investigated and discussed.

The LI curves of the embedded VCSEL's and photodiodes were measured to define which optical power is emitted by the VCSELs and detected by the photodiodes. This allowed us to define the total optical loss of an embedded link by monitoring the VCSEL and PD currents. Different measurements were performed to define the major contributors to the total optical link loss and to compare the use of laserablated mirrors and mirror plugs. The total optical link loss using laser ablated mirrors is 20 dB $\pm$ 7 dB, and using mirror plugs: 6.4 dB $\pm$ 1.5 dB. For laserablated mirrors, most of the optical power is lost by vertical out-coupling at the VCSEL mirror facet. For mirror plugs, we measured that about 63% of the loss is found in the VCSEL side of the link and 37% at the PD side. The metallization of laser ablated mirrors with a vapor deposited gold layer increases the optical loss for 1.4 dB per mirror facet for a reason which still needs to be defined. Crosstalk measurement showed a cross-talk of -34 dB between two neighboring 8 cm long planar waveguides and -17 dB between two neighboring VCSEL-to-PD links.

The investigation on the flexible behavior taught us that the flexible optical waveguide foil can be bended over 1000 times over a bending radius of 2.5 mm without damaging. A foil with embedded and galvanic interconnected VCSEL's and photodiodes was successfully bended over 1000 times over 2.0 mm bending radius cylinders without any chance in functionality or VI curve of the VCSEL or PD. The complete stack of embedded opto-electronics and waveguides however shows poor flexibility.

A special electronic design on an rigid optical embedded link was made and fabricated with SMA and SMD components to allow us to do time and frequency domain characterization at high-speed/high-frequency using standard 50 Ohm test equipment, without requiring a VCSEL driver to drive the VCSEL's and without requiring a trans-impedance amplifier for the photodiodes. After shielding, grounding and wiring the optical link sample, it was connected to a pattern generator resulting in a clear open eye diagram at 1.2 Gb/s.

The reliability of the flexible optical link was investigated through storage, heat cycling and humidity tests. Temperature cycling and humidity storage was performed on both rigid optical links on FR-4 and on flexible optical links. The rigid optical links delaminated from the FR-4 substrate when the temperature reached -30 ^{o}C and their total optical losses increased with the humidity exposure time. The flexible optical links did not degrade at all after 100 temperature cycles between -40^{o}C and + 125^{o}C and after 1000 hours at 85 ^{o}C at a relative humidity of 85 %. Exposing the optical links to a solder reflow temperature profile which reaches about 250 ^{o}C for 30 seconds, deforms the shape of the foil and increases the total optical link foil with 1.3 dB, which is acceptable. The deforming of the foil can be avoided in several ways.

VCSEL's can generate a lot of heat which can shorten the VCSEL lifetime and cause incorrect functioning. Especially, the heat spreading of embedded VCSEL's can become a real problem. Thermal simulations using a 2D cross-sectional model showed that the thinner the foil is, the worse the heat spreading will be. Scaling the heat sink size can compensate for this. Because the heat distribution is uniform over the thickness of the complete foil, a thin plate model was used for further simulation. This approach results in a more accurate approximation of the absolute temperature. A 1 x 4 VCSEL array with all VCSEL's dissipating maximum power in continuous mode, the VCSEL temperature can raise upto 220^{o}C for a 3 x 1.2 mm^2 heat sink and upto 80^{o}C for a 16 x 2.4 mm^2 heat sink size. The latter is an acceptable temperature, since the average dissipated power by the VCSEL will be much lower than the absolute maximum. When opening the heat sinks with laser ablation and electroplating the foil at the backside, the heat sink can have the same size as the substrate itself.

Optical characterization and comparison of wirebonded VCSEL's and embedded VCSEL's shows that the embedding does not influence the optical behavior of the VCSEL's.

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Chapter 9

Conclusions and Outlook

This chapter presents an overview of the main achievements within this PhD work and a brief look into the opportunities of future work.

9.1 Main achievements

The main objective of this PhD was the embedding of opto-electronics and optical waveguides inside a flexible foil. The integration of these features inside a polymer thin foil implies the need for ultra thin opto-electronics, embedded optical coupling elements and galvanic interconnections.

The requirements for the foil material were unraveled in terms of flexibility, optical transparency and process compatibility. A study on the state-of-the-art materials revealed the fact that only optical waveguide materials are available for rigid applications, while those for flexible applications have been developed and reported, but remain commercially unavailable. Therefore we chose to work with commercially available non-flexible materials (Truemode™ Backplane Polymer , LightLink™ , Epocore / Epoclad and Ormocers®). The flexibility of these non-flexible materials can be significantly enhanced by using mechanical support layers. As an ongoing alternative, modifications are being made to these existing materials to improve their flexibility in close cooperation with the PBM Group of the Ghent University.

The process flows for the fabrication of optical waveguides in Truemode™ Backplane Polymer , LightLink™ , Epocore / Epoclad and Ormocers® material was optimized in function of waveguide profile, waveguide roughness and dimensions. An analysis of dimensional short term and long term variations was

made in the scope of embedding active components and coupling elements later on in the research, were positioning requirements become very strict. Especially planarization of the different spincoated materials was characterized. Process problems like edge bead, adhesion issues, air bubble insertions, proximity mode UV exposure and waveguide T-topping were studied and tackled within the possibilities.

Since the optical waveguide material is not flexible, techniques have been investigated to support the waveguide layers mechanically at top and bottom with Polyimide layers. A first approach consists of the lamination of a waveguide layer stack in between two Polyimide foils. Therefore a peel-off technique and a sacrificial layer release method was developed to release the optical waveguides from their temporary rigid processing carrier and laminate them afterwards. In a second approach, the optical waveguide stack was sandwiched in between two identical spincoated Polyimide layers which were processed in the same process flow as the waveguide stack. A dedicated adhesion promoter approach enabled us to release the complete stack afterwards by laser ablation. The resulting waveguide foils were investigated for their flexibility and optical bending propagation losses. The Truemode™ Backplane Polymer material showed superior bending behavior over the other materials with a minimum bending radius lower than 2.5 mm tested for 1000 bending cycles. The bending losses of the LightLink™ and Truemode™ Backplane Polymer materials showed to be comparable to those reported in literature.

Commercially available opto-electronic components are too thick to be embedded inside a thin foil. Within this PhD work, a backside lapping and polishing process was developed to thin down individual VCSEL and photodiode arrays to a thickness of only 20 μm . Mechanical stress inside the GaAS dies was minimized by reducing the backside roughness to 10 nm rms, measured on an area of 200 x 200 μm^2. The flatness of the final thinned dies is below 2 μm due to the optimization of the wax-mounting and the lapping tool maintenance. The thinning process was proven to be scalable to GaAs chips upto a size of 10 x 10 mm^2. Electrical and optical characterization of thinned VCSEL's showed that the removal of the backside substrate does not affect its functional behavior.

The embedding of the thinned opto-electronic components inside the cladding layer of the flexible optical waveguide foil was investigated using different polymers as embedding material. Each embedded chip is provided with a copper plated heat sink and was leveled with the embedding layer. Laser ablated microvia's and a sputtered copper layer provide galvanic interconnection towards the embedded chips and fans out the small pitch chip contact pads towards larger contact pads if necessary. These can be opened using different laser ablation steps and can be used for soldering and galvanic contact to the outer world. Together

with the opto-electronics, we achieved to embed ultra thin Integrated Circuits (IC's) in the same layer to enhance the intelligence of the foil. The waveguide stack which needs to be fabricated on top can be aligned with a 10 μm accuracy.

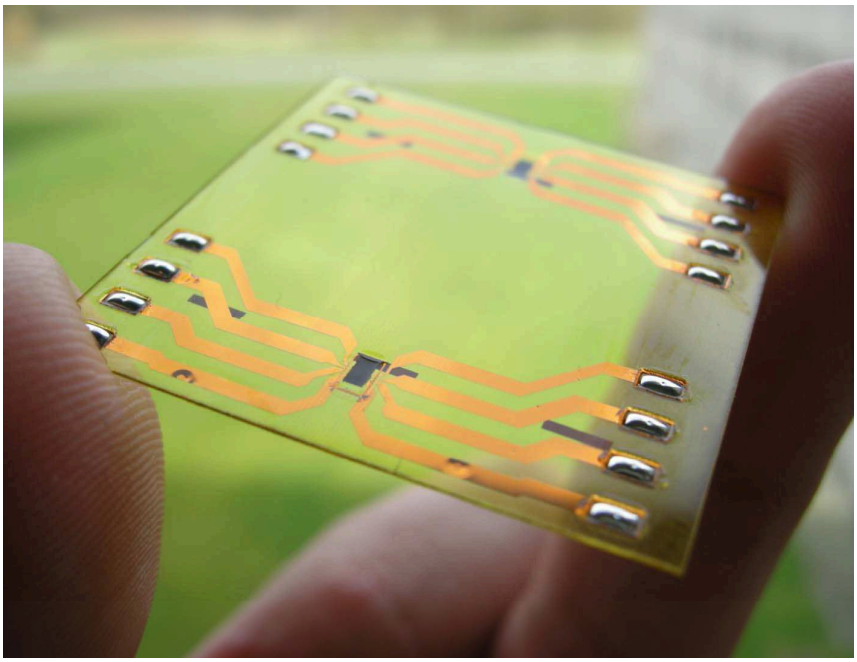

Figure 9.1: Picture of a 180 μm thin foil with embedded VCSEL-to-PD links and galvanic interconnections.

VCSEL's / Photodiodes are vertically emitting / detecting actives, which introduces the need for out-of-plane coupling towards the horizontal waveguides. The use of laser ablated micro-mirrors and pluggable mirror inserts has been investigated thoroughly. Ray tracing ZEMAX simulations were performed on the embedded optical link build-up to define the main dimensional contributors to the total optical loss of the system. The evaluation of laser ablated mirrors revealed three main drawbacks: insufficient depth control, alignment accuracy and mirror flatness. A process for the fabrication of pluggable micro-mirrors was presented using a 45 degree polishing approach resulting in mirror surfaces with a $\pm$ 1 degree angle accuracy and with a coupling efficiency of about 90%. Alternative fabrication methods like Wire-EDM and Deep Proton Writing (DPW) were also investigated. The mirror plug components were integrated and aligned with 10 μm accuracy inside the layer build-up which couple the light from the waveguides to the opto-electronics. Optical communication from and towards the foil with optical fibers was made possible by embedding and aligning single bare

optical fibers inside the foil, eliminating the need for a bulky, rigid connector unit.

Characterization of the embedded optical link foil as a total system (see Figure 9.1) was performed by means of the optical power budget, optical crosstalk, high-frequency behavior, mechanical flexibility, reliability and heat management. Different measurements set-ups were assembled to define the major contributors to the total optical link loss and to compare the use of laser ablated mirrors and mirror plugs. The total optical link loss using laser ablated mirrors is 20 dB $\pm$ 7 dB, and using mirror plugs: 6.4 dB $\pm$ 1.5 dB. Crosstalk measurements showed a cross-talk of -34 dB between two neighboring 8 cm long planar waveguides and -17 dB between two neighboring VCSEL-to-PD links. The investigation on the flexible behavior taught us that the flexible optical waveguide foil can be bended over 1000 times over a bending radius of 2.5 mm without damaging. A foil with embedded and galvanic interconnected VCSEL's and photodiodes was successfully bended over 1000 times over 2.0 mm bending radius cylinders without any chance in functionality or VI curve of the VCSEL or PD. The complete stack of embedded opto-electronics and waveguides however shows poor flexibility. A special electronic design on an rigid optical embedded link was made to do time and frequency domain characterization using standard 50 Ohm test equipment resulting in a clear open eye diagram at 1.2 Gb/s.
The reliability of the flexible optical link was investigated through storage, heat cycling and humidity tests. Temperature cycling and humidity cycling was performed on both rigid optical links on FR-4 and on flexible optical links. The rigid optical links delaminated from the FR-4 substrate when the temperature reached -30 ^{o}C and their total optical losses increased with the humidity exposure time. The flexible optical links did not degrade at all after 100 temperature cycles between -40^{o}C and + 125^{o}C and after 1000 hours at 85 ^{o}C at a relative humidity of 85 %.
The thermal management of embedded VCSEL's was analyzed with a 2D cross-sectional model and a thin plate model. Main conclusion is the trade-off between heat-spreading versus total foil thickness: the thinner the foil, the worse the heat spreading. Scaling the heat sink size can compensate for this. When opening the heat sinks with laser ablation and electroplating the foil at the backside, the heat sink can have the same size as the substrate itself.
Optical characterization and comparison of wirebonded VCSEL's and embedded VCSEL's shows that the embedding does not influence the optical behavior of the VCSEL's.

9.2 Future work

9.2.1 Future substrate material

The technologies described in this work are open for further optimization and adjustments according to the aimed application. The major optimization would be the mechanical flexibility of the active optical foil. To improve this characteristic, layer thicknesses of the stack could be reduced to a minimum with further optimization. A much more robust approach would be the material choice. In Chapter 2, we discussed a range of materials with excellent bending properties but which are still commercially unavailable. Negotiations are however ongoing between CMST Microsystems and a few of the providers, which could result in the availability of flexible optical material in the near future. Optimization of process parameters and reliability tests with the new materials should be considered. As an ongoing alternative, modifications are being made to the existing commercially available materials to improve their flexibility in close cooperation with the PBM Group of the Ghent University.

The fabrication process of the fully embedded optical link as presented in this PhD thesis uses quite expensive materials and processing techniques. Looking into mass production deposition and structuring techniques could result in cheaper solutions. Replacing the Polyimide supporting layers with cheap substrates like PEN and PET can also bring the cost significantly down. These approaches are being investigated in the ongoing PhD research of MSc. Sandeep Kalathimekkad at CMST Microsystems.

9.2.2 Demonstration

In the Introduction Chapter 1, we analyzed the feasible application market of the active flexible optical link. To narrow the gap between technology and application, future work should involve the realization of well-considered demonstrators:

The demonstration of the active flexible optical link in portable applications for high throughput data communication demands for more intelligence and signal conditioning within the foil. Therefore, a next generation demonstrator of the embedded optical link would be a total system integration of VCSEL's, photodiodes, VCSEL drivers and trans-impedance amplifiers inside the SU-8 layer of the active optical foil. The technology to thin down these components has been presented in this work (Chapter 5) for GaAs chips and in [1] for Si chips. The embedding of the opto-electronics and the electronics inside the SU-8 layer was presented in Chapter 6, Section 6.2 and the electrical interconnection of them all

in Chapter 6 Section 6.4. This means all the technologies are available to realize such a demonstrator in future work. Figure 9.2(top) shows the cross-sectional build-up and an alternative with the use of UTCP's (bottom). This alternative consists of the separate packaging of drivers and amplifiers inside a flexible Ultra Thin Chip Package (UTCP [1]) and laminate them on top of the active opto-electronic foil. Standard through-via's and metallization steps can interconnect the UTCP's with the embedded opto-electronic components.

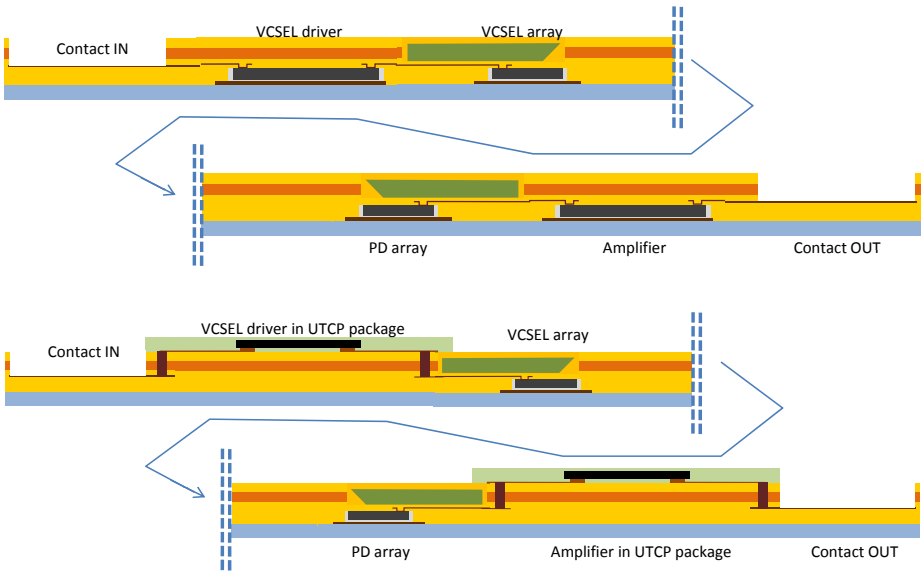

Figure 9.2: Next generation demonstrator principle with VCSEL drivers and trans-impedance amplifiers

The demonstration of the embedded optical links in the world of optical sensing is ongoing in the PhD researches of Ir. Jeroen Missinne and Bram Van Hoe at CMST Microsystems. Both works are carried out in the framework of the FAOS project [2] and the Phosfos Project [3], which are described in more detail in Chapter 1, Section 1.4. Three demonstrators are put forward in these projects:

- A first demonstrator consists of the embedding of fibers with fiber Bragg gratings in a skin compliant stretchable foil [4]. The light sources, detectors and electronic circuitry are embedded or integrated on compact flexible signal processing boards which are then mounted and coupled with the compliant optical sensing skin.
- A second demonstrator is a novel type of pressure sensor based on optical feedback in a VCSEL [5]. A moveable external cavity with reflector is used

to implement the optical feedback mechanism. The pressure sensor is realized by embedding a thinned array of semiconductor lasers in a thin flexible foil. It is possible to fabricate a fully integrated sensor with a dense matrix of pressure sensitive points. A resolution of half the VCSEL wavelength can be obtained.

- The third demonstrator is a high density optical pressure sensor based on a matrix of 2 stacked layers of crossing multimode waveguides [6]. These 2 layers are separated by integrated spacer structures to produce a gap between the waveguide layers when the sensor is idle. When pressure is applied on such a sensing element, the distance between the waveguides from the upper and lower layer will decrease and power is transmitted between these waveguides. The sensor consists of polymer waveguides embedded in polydimethylsiloxane (PDMS) which is a very flexible material. Therefore, it is ideally suited to use as artificial skin. The light sources and detectors are integrated in a flexible foil and are then mounted and coupled with the stretchable optical waveguides.

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